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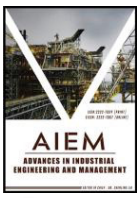

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RESEARCH ARTICLE

DESIGN OF LOW POWER HIGH SPEED DOUBLE TAIL COMPARATOR WITH 45NM TECHNOLOGY FOR ADC APPLICATION

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ABSTRACT

In the present scenario low power and high speed play a significant role specifically in the field of VLSI circuits. Comparator is one of the major parts of an analog to digital converter (ADC) that can improve the overall performance of Flash/Pipeline Analog to Digital Converter.The main objective of this paper is to design and implementation of different comparator and compared in terms of power consumption, propagation delay and transistor count. The results of this paper are simulated on the EDA tanner tool realized in 45-nanometer technology at 1v supply voltage. Simulation result shows that the proposed-2 comparator has low power dissipation of 8.63 microwatt with high speed of 3.41GHz.

KEYWORDS

Comparator, Double-Tail Comparator, Analog to Digital Converter, Low power, High speed, Transistor Count, Tanner EDA.

1. INTRODUCTION

The power consumption is a vital issue in CMOS circuits, where different architectures and technologies are used to design circuits for low power dissipation with small size and high-speed interface applications are developed. In mixed signal integrated circuits analog to digital converter is one of the most important component which has required low power, high speed and high resolution. High-speed comparators in ultra deep sub micrometer (UDSM) CMOS technologies be afflicted by low supply voltages [1].

In advanced technology designing of high speed comparator with low supply voltage is the more challenging issue [2]. Now-a-days ADC's are widely used in hard disk drives, digital video discs and local area networks. In mobile and portable devices where analog to digital converter is used which has required low power dissipation, low noise ,high speed, less hysteresis , less Offset voltage.

Circuit size relies on upon the quantity of transistors and their sizes and on the wiring complexity, where the wiring complexity may fluctuate significantly from the one architecture to another. In this paper, CMOS dynamic latch comparator is designed using different architecture with the low power consumption and high speed in 45-nanometer technology at 1v supply voltage.

2. ANALOG COMPARATOR

Analog comparator compares two current or voltage signals where one signal is the input signal and another is the reference signal and after the comparison of these two signals it will produce a digital output. Analog comparator is one of the fundamental building blocks in most analog -to-digital converters (ADCs). Many high speed ADCs, such as flash ADCs, require high speed low power comparators. It has two analog input terminals V+ and V- and one binary digital output V0. The block diagram of analog comparator seems in Figure 1. The output is ideally

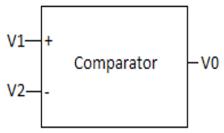

Figure 1: Block diagram of analog comparator.

$$V0 = 1, \text{ if } V+ > V-$$
$$= 0, \text{ if } V+ < V- \quad (1)$$

An analysis about the power consumption and speed has been verified for various architectures.

3. LITERATURE REVIEWED

Over the past few years' researchers has designed analog comparator by using some excellent thoughts.

A dynamic latch comparator has been designed with the aid of Jeon and Kim [3]. It can reduce latch offset voltage and delay. power consumption & hysteresis response. Simulation is done by 90nm technology at 1V supply voltage. Offset voltage is reduced by 19% and delay is reduced by 62% than conventional comparator.

A CMOS comparator has been designed by Smriti Shubhanand, Rao [4]. It provides high speed and low propagation delay. It can reduce latch offset voltage & power consumption & hysteresis response. Here, supply voltage is 1v. Propagation delay achieved is 1.787ns. Here 0.25µm

technology is used.

Bao-ni Han, Yin-tang Yang, Zhang-ming Zhu [5] presented, based on pre-amplifier latch theory, composed pre-amplifier includes positive & negative resistance connected in parallel as its load, a regenerative latch & simple output stage. Power supply is 1.8v, maximum offset voltage is 0.6mv and high clock frequency is 1.25GHz. Here 0.18µm technology is used.

Dhanisha N. Kapadia [6] presented, design of a CMOS charge sharing dynamic latch comparator along with the buffer stage in 130nm and 90nm technologies. The propagation delay is the time required to the change in output with respect to the change in input. Supply voltage is 1.3v and 0.9v, Propagation delay achieved is 2.13ns & 0.75ns for 130nm & 90nm technology respectively.

Samaneh Babayan-Mashhadi [1] has been designed a new technique based dynamic comparator with low power and low voltage functionality. Here 0.18µm technology is used for the simulation purpose. This proposed comparator offers better overall performance than other comparators.

Sivasathya and Manikandan [7] has been designed a SAR using double-tail comparator which is applicable in all types of ADC's for high speed applications. The simulation is done in microwind software 3.1.

Bhuvaneswari, Gowrishankar, and Dr. Venkatachalam [8] has been designed of existing clocked dynamic comparators in different scaling technologies. This paper shows that the HSDC design provides better delay reduction compared to conventional dynamic comparator design.

Monica Rose Joy [9] presented the dynamic comparator using proposed technique. In this technique few numbers of transistors are included to improve the strength of positive feedback which reduces the delay and power at low supply voltage.

Madhumathi, Ramesh Kumar [10] presented a paper on dynamic comparator. The proposed comparator reduces offset voltage, delay, power and provides high speed [11-16]. The proposed comparator can be used for high speed ADCs. 0.25µm technology is used. Here the supply voltage is 0.8v and the frequency is 41MHz.

4. CONVENTIONAL ANALOG DYNAMIC COMPARATOR

In the present situation low power and high speed are imperative factors in the field of VLSI circuits. The conventional dynamic comparator [1], [11] appears in Figure 2. Positive feedback mechanism is used in dynamic latch comparator to regenerate the input signal into a full scale digital level output signal [12]. In this architecture Mtail transistor control the current flow between the differential pair input transistors M1 and M2 and the latch formed by M3 and M6. During the reset phase once clock is zero and Mtail is off, hence both output nodes Outn and Outp charged to VDD by the transistors M7 and M8 to define a start condition. In the decision making phase, the output voltages Outn and Outp begin to discharge with different discharging rate relating to the input voltages INN and INP. If the input voltage INN is greater than INP, then the output voltage Outn is discharge faster than Outp. So Outn falls down to (VDD – V_{th}) before Outp, as a result transistor M6 is on. Thus Outp charged to VDD and Outn is discharged to ground. If the input voltage INP is greater than INN, then Outn charged to VDD and Outp is discharged to ground.

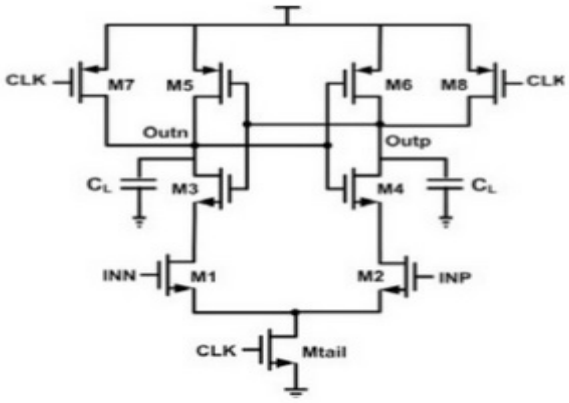

Figure 2: Architecture of Conventional dynamic comparator.

5. CONVENTIONAL DOUBLE-TAIL DYNAMIC COMPARATOR

The conventional double-tail dynamic comparator [13] is shown in Figure 3. This type of comparator has an advantage over the previous one is the less stacking effect and lower supply voltage is required to operate it. Transistor Mtail1 and Mtail2 are inactive when clock pulse is in low logic level, fn and fp nodes are charged to VDD through the transistors M3 and M4. Subsequently MR1 and MR2 transistors reset both latch output to ground. In the decision making phase both the transistor Mtail1 and Mtail2 are in on condition, fn and fp node voltages start to fall with different rates according to the input voltages and drain current of transistor Mtail1. If the input voltage INP is greater than INN, then fn is discharging more quickly than fp through Mtail1. The output node Outn will be discharged to the ground through the transistor M9, leading transistor M8 to turn on and another output node Outp will be charged to VDD.

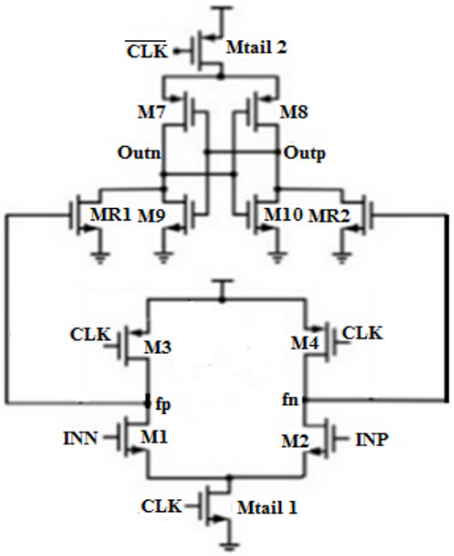

Figure 3: Conventional double tail dynamic comparator.

6. PROPOSED -1 DOUBLE-TAIL DYNAMIC COMPARATOR

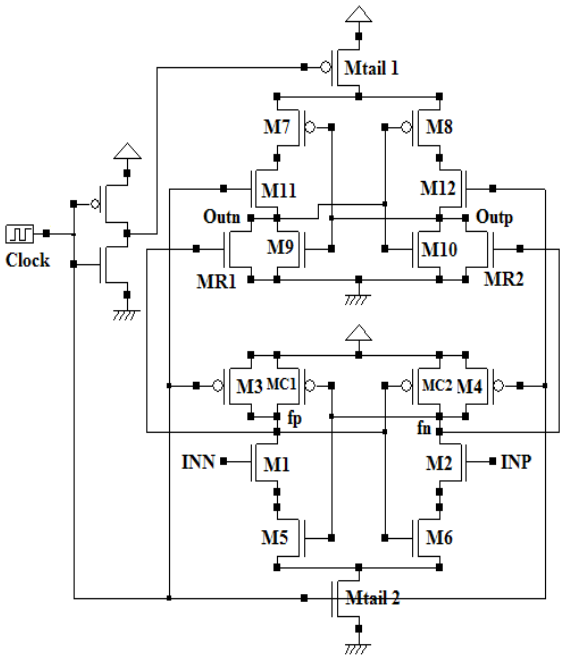

Figure 4: Architecture of Proposed-1 dynamic comparator.

The architecture of this comparator is shown in Figure 4. Throughout the reset section, each transistor Mtail1 and Mtail2 are in off circumstance, fn and fp nodes are charged to VDD through the transistors M3 and M4. Finally MR1 and MR2 transistors reset each latch output to ground. In the decision making section, fn and fp node voltages begin to fall with different rates according to the input voltages If the input voltage INP is greater than INN, then fn will be discharged more quickly than fp. Therefore the transistor MC1 to turn on which will charge node fp to VDD. As the node fp charged to VDD, the transistor MC2 will turn off and the transistor M5 will turn on, therefore the node fn will be discharged completely. The output node Outn will be discharged to the ground through the transistor M9 and MR1, leading transistor M8 to turn on and another output node Outp will be charged to VDD. M11 and M12 work as switches embedded in cross coupled inverter pairs made of M9-M7 and M10-M8. The purpose of using M5 and M6 transistors just below the input transistors is to reduce the static power consumption.

7. PROPOSED-2 DOUBLE-TAIL DYNAMIC COMPARATOR

The proposed-2 double-tail dynamic comparator is appeared in Figure 5. Transistors M3 and M4 are in operating condition when clock pulse is in low logic level, therefore fn and fp nodes are charged to VDD. M13 and M14 transistors are cut off. Subsequently MR1 and MR2 transistors reset both latch output to ground. In the decision making phase, transistors M3 and M4 turn off. Thus fn and fp node voltages are discharge with different rates according to the input voltages. If the input voltage INP is greater than the input voltage INN, then fn will be discharge more quickly than fp, because more current will flow through the transistor M2 than the transistor M1. Therefore the transistor MC1 to turn on which will charge node fp to VDD. As the node fp charged to VDD, the transistor MC2 will turn off and the transistor M5 will turn on, therefore the node fn will be discharged completely. Hence the transistor M13 is turn off and M14 is turn on. The output node Outn will be discharged to the ground through the transistor M9 and MR1, leading transistor M8 to turn on and another output node Outp will be charged to VDD. M11 and M12 work as switches embedded in cross coupled inverter pairs made of M9-M7 and M10-M8. M5 and M6 transistors are used to reduce the static power consumption.

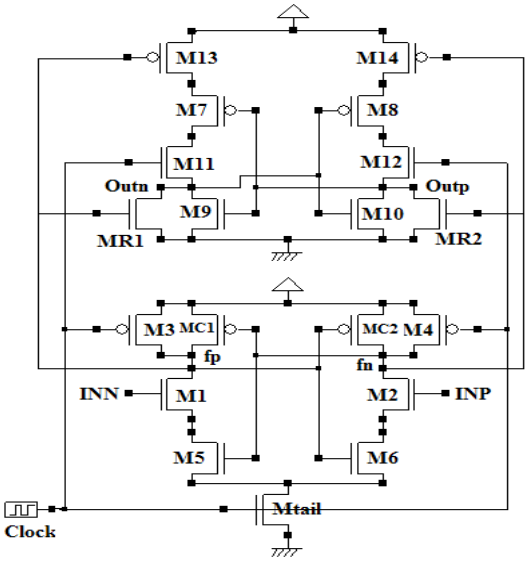

Figure 5: Architecture of Proposed-2 dynamic comparator.

8. SIMULATION RESULTS

To compare the performance of different type of comparators in terms of power consumption, speed and transistor count, EDA tanner tool has been used in 45-nanometre technology with 1v supply voltage for design and implementation of all circuits. The schematic circuit diagram of conventional dynamic comparator, conventional double-tail dynamic comparator, and proposed-1 and proposed-2 comparator are appearing in Figure 6, 7, 8 and 9 respectively. The output waveform of proposed-2 comparator is appearing in Figure10. Layout of proposed-1 and proposed-2 dynamic comparator is shown in Figure 12 and 13 respectively. The performance comparison of different types of dynamic comparator is abridged in Table 1. The performance comparison of proposed-2 dynamic comparator using different technology is shown in Table 2.

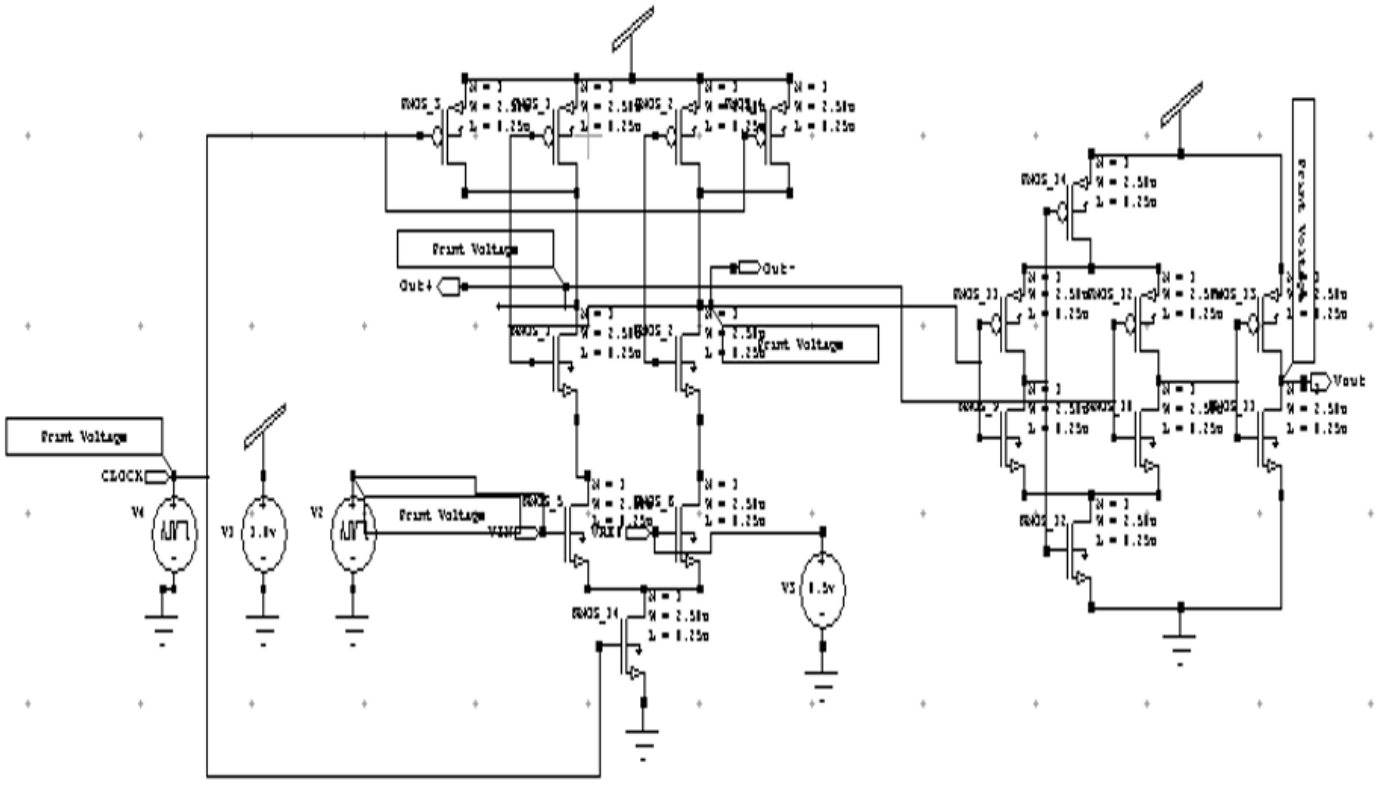

Figure 6: Schematic of conventional dynamic comparator with output buffer circuit.

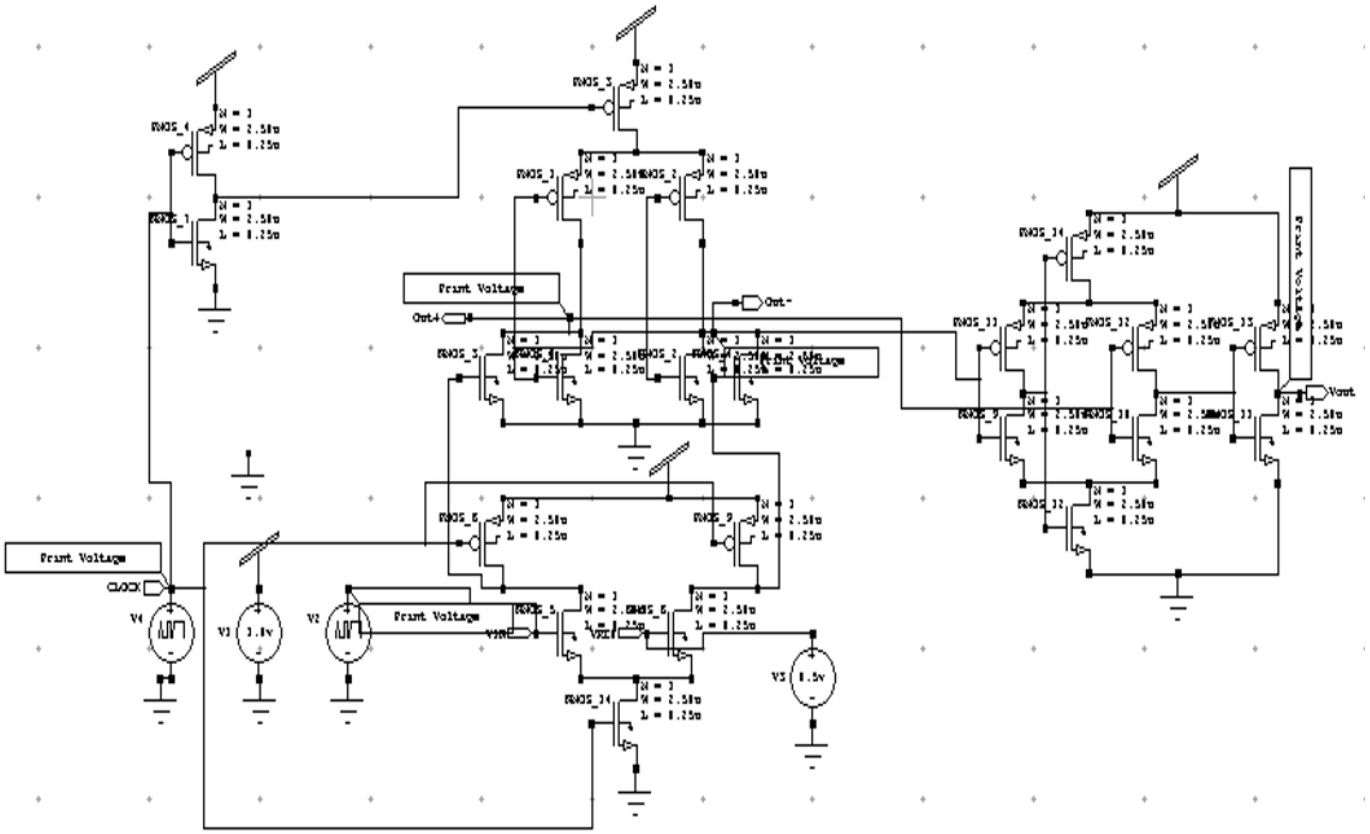

Figure 7: Schematic of conventional double tail dynamic comparator with output buffer circuit.

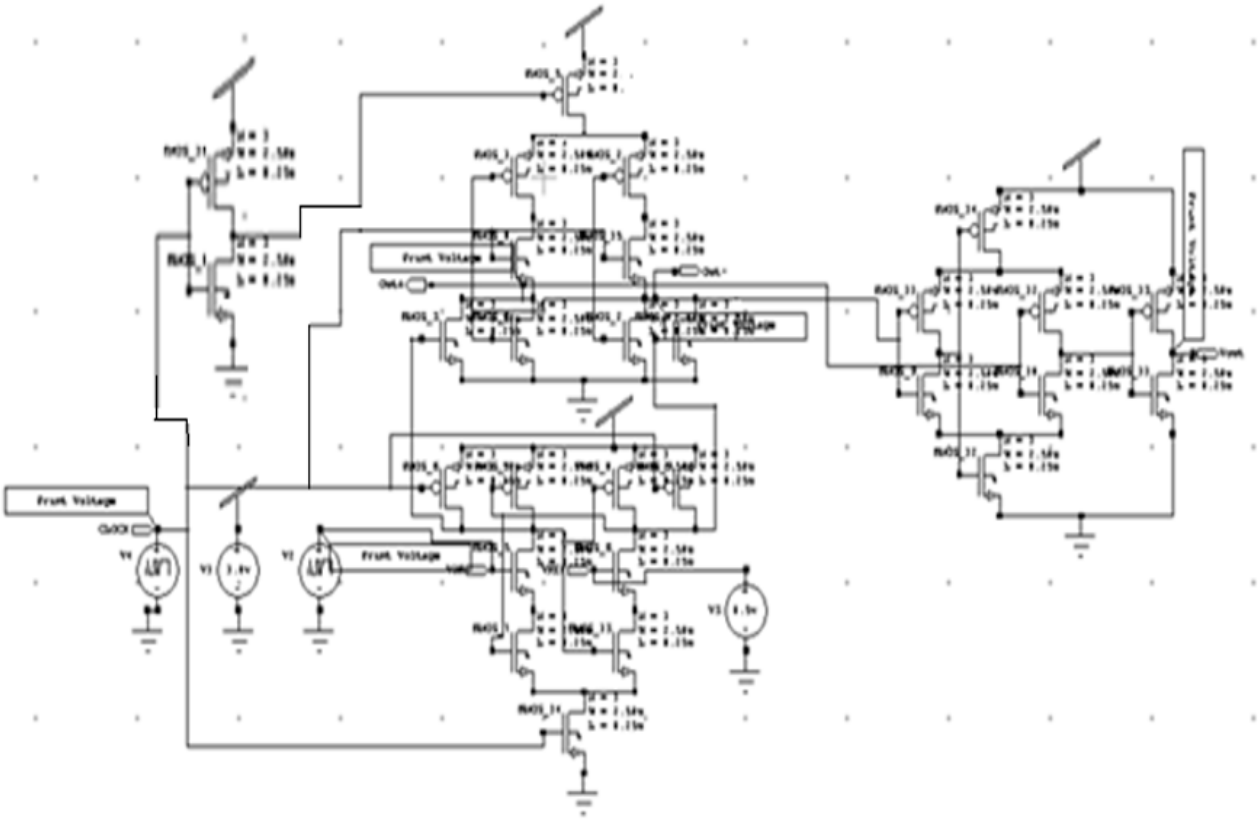

Figure 8: Schematic of proposed-1 double-tail dynamic comparator with output buffer circuit.

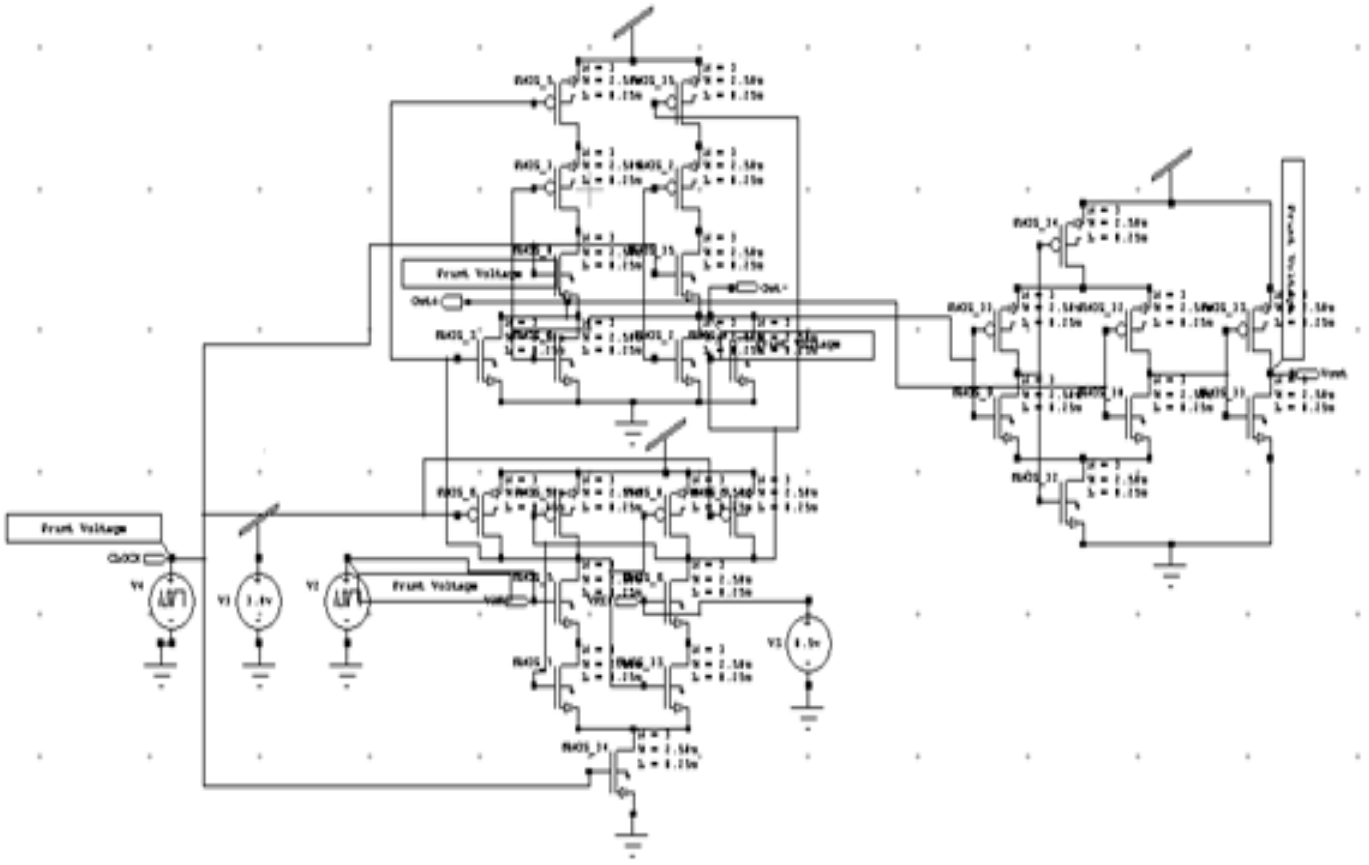

Figure 9: Schematic of proposed-2 double- tail-dynamic comparator with output buffer circuit.

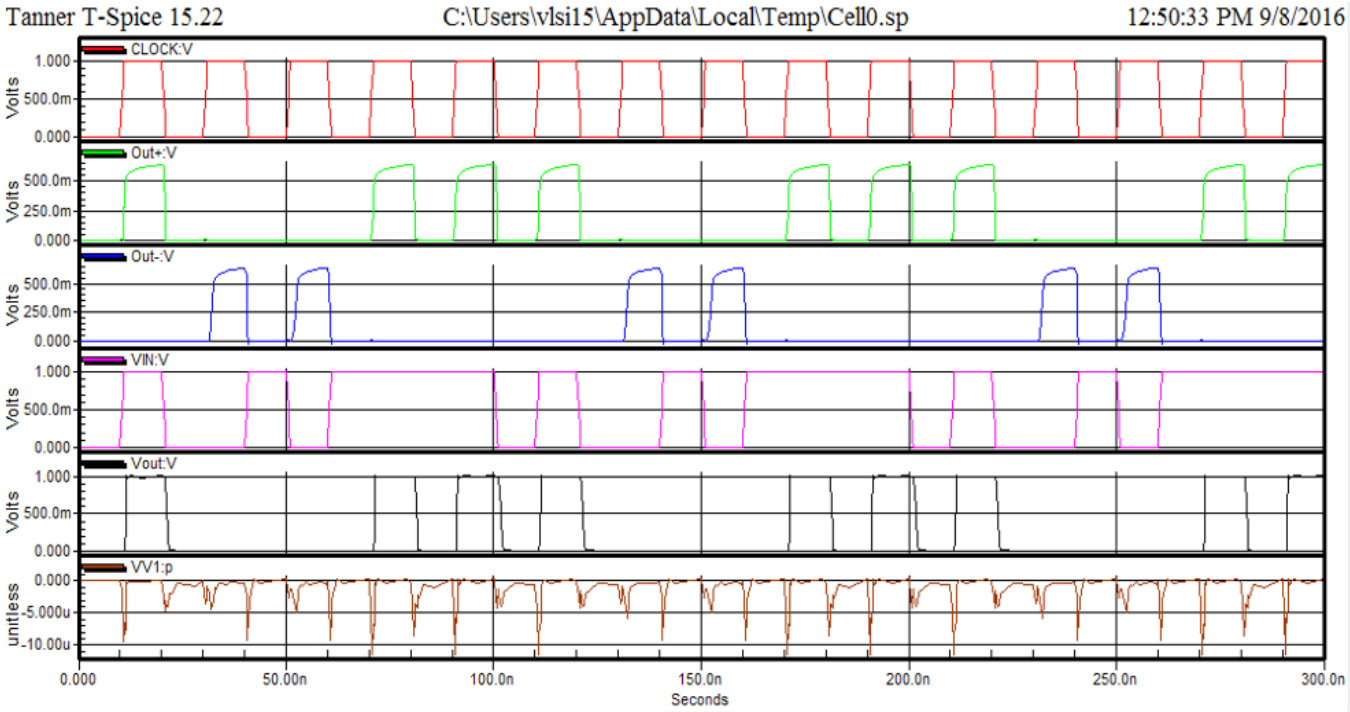

Figure 10: Output waveform of proposed-2 comparator.X

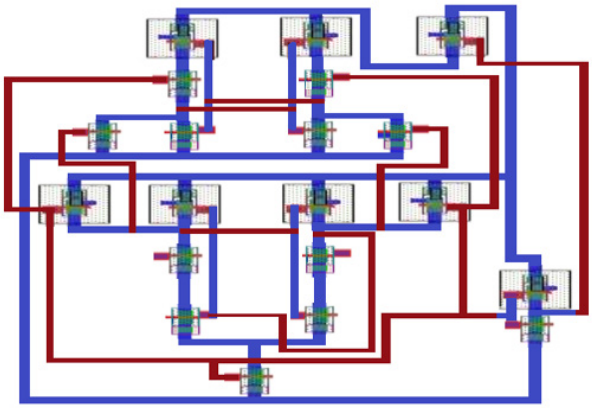

Figure 11: Layout of proposed-1 comparator.

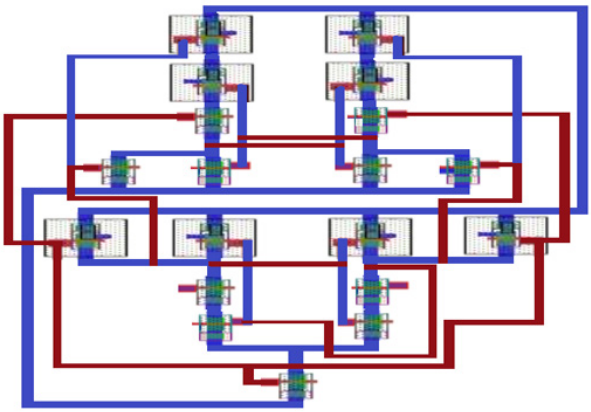

Figure 12: Layout of proposed-2 comparator.

Table 1: Performance comparison of dynamic comparators.

Comparator	Transistor count	Power dissipation (μW)	Propagation delay (n-s)	PDP (μ-nJ)	Speed (GHz)
Conventional Dynamic Comparator	17	16.41	0.446	7.31	2.24
Conventional Double -Tail Dynamic Comparator	22	13.12	0.347	4.55	2.88
Proposed -1 double tail dynamic comparator	28	9.06	0.308	2.79	3.24
Proposed -2 double tail dynamic comparator	27	8.63	0.293	2.52	3.41

Table 2: Performance comparison of proposed-2 dynamic comparator using different technology.

Parameters	250nm	180nm	130nm	45nm
Power consumption (μW)	10.92	9.81	9.41	8.63
Propagation delay (n-sec)	1.04	0.85	0.64	0.29
Speed (GHz)	0.96	1.17	1.56	3.41

9. CONCLUSIONS

After design and Simulation of all type of analog comparator it is found that proposed-2 dynamic comparator has better performance than other comparators. Power utilization of the proposed-2 dynamic comparator is 34.22% less than the conventional double tail dynamic comparator and it will operate at high speed of 3.41 GHz.

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