Study of characteristic parameters for Channel and Gate Engineered Double Gate MOSFET considering Gaussian doping and Inner Fringing Capacitance

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Abstract: An analytical expression of subthreshold Surface Potential, Drain Current and Threshold Voltage is formulated for Double Halo Dual Material Double Gate(DHDMDG) MOSFET taking into account Inner Fringing Capacitances at the Source and Drain end. The doping profile concentration considered for the halo regions at the source and the drain end is Gaussian in nature. The results of Ten from the proposed model are compared with those from the models of Channel Engineered conventional MOSFET structure. It is found that DHDMDG structure suppresses short channel effects more effectively as compared to conventional MOSFETs. Very good agreement of the proposed result obtained from the models of DHDMDG with those from DESSIS validates the model in suppressing short channel effects.

Keywords: Gaussian Doping; Inner Fringing Capacitance; Channel Engineering; gate Engineering; Double Gate MOSFET.

1 INTRODUCTION

Advancement of CMOS technology has led us to a period where dimension of MOSFET have continued to shrink to achieve an improved performance, particularly in the dynamic power dissipation and higher packing density and to make MOSFETs work in a higher speed and properly as well. Nowadays large scale integration has improved the processing speed by using more number of MOSFET in a CMOS design and in turn, it has given rise to a significant increase in leakage current due to subthreshold conduction and the shrinking process has caused some effects known as "Short Channel Effects(SECs)" in MOSFETs [1,2,3]. Due to several undesirable phenomena which includes effects like Hot Electron Effect, DIBL, Punch through, Threshold Voltage roll-off, Velocity Saturation, Surface Scattering etc. Desirable performance and speed with undesirable effects on reducing the IC size by increasing the number of transistor have become the challenge for the modern and advanced technological devices. One of the most effective solutions of those undesirable effects is to use Halo and Gate Engineering techniques where Two or more Gates with two or more materials have been used in the

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MOSFET designing. When the channel length is below 50 nm, double gate MOSFETs are seen to be most effective due to their immunity power to Short Channel Effect(SECs). Scaling of device leads to significant increase of fringe capacitance, which often dominates the total capacitance. MOSFETs'

performances get degraded by this kind of parasitic effects and therefore Modeling of devices should be considered to reduce this kind of effects. Fringing fields play a vital role in the variation of surface potential leading to an increased electric field. Halos are pocket implants situated at the source and drain regions which are nothing but highly doped region compared to the substrate [4,5,6]. An accurate fringing model of subthreshold potential with double halo regions have been proposed for short channel Double Gate MOSFET in this paper.

In this paper, an analytical expression of subthreshold surface potential, threshold voltage and drain current is proposed for channel and Gate Engineered Double Gate MOSFET considering Gaussian Doping concentration in the two halo regions at the source and the drain end and inner fringing capacitance effect. It is seen that the model results tally effectively with those from DESSIS, validating the models for suppressing Short Channel Effects.

2 MODEL DESCRIPTION

The structure of Double Halo Dual Material Double Gate (DHDMDG) MOSFET, Double Halo Single Material Double gate (DHSMDG) MOSFET and Single Halo Single Material Double gate (SHSMDG) MOSFET are shown in Fig 1,2 and 3.

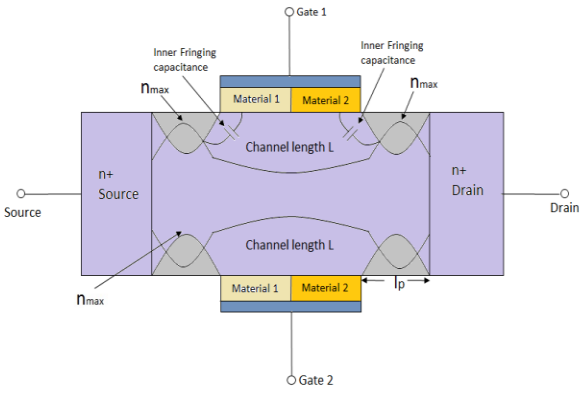

Fig 1: Double Halo Dual Material Double Gate(DHDMDG) MOSFET

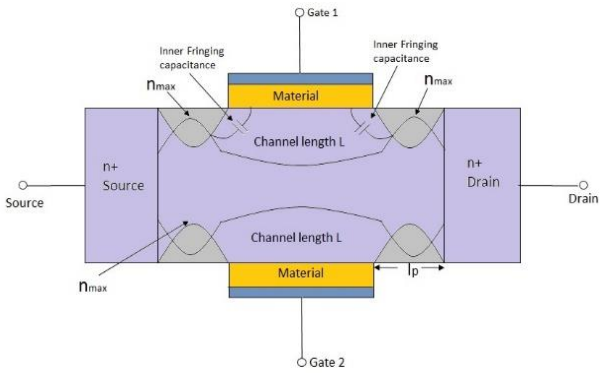

Fig 2: Double Halo Single Material Double Gate(DHSMDG) MOSFET

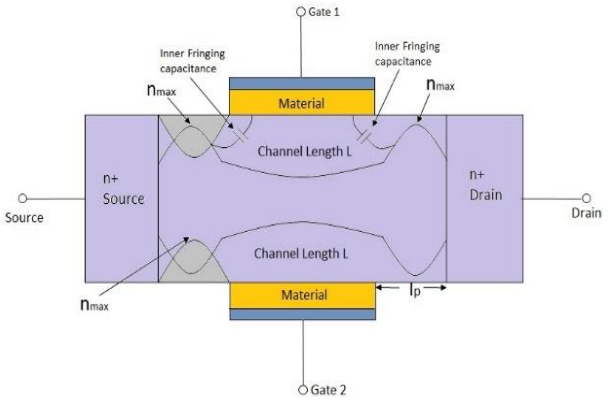

Fig 3: Single Halo Single Material Double Gate(SHSMDG) MOSFET

A rectangular box of length Δx, at a given channel length x is considered, which can give the analytical expression of Subthreshold surface potential by covering the entire depletion region width Y_{dGauss} and $W_{dthGauss}$ [1,2]. Since the device has two gates, the vertical electric field components E_{Gate1} on the top or front side and E_{Gate2} on the bottom or back side are both non-zero. So, we can obtain E_{Gate1} and E_{Gate2} from the potential balance equations as follows:

$$V_{gbf} = V_{fbf} + \psi_{subSP} + \psi_{ox} V_{gbb} = V_{fbb} + \psi_{subSP} + \psi_{ox} \quad (1)$$

For the bottom gate,

ψ_{subSP} = Surface potential, as the potential drop from the surface to the bulk outside the depletion region

Ψ_{ox}= Potential drop across oxide layer

V_{gbf} = Front gate bias voltage

V_{gbb}= Back gate bias voltage

V_{fbf}= Flat band voltage under front Gate

V_{fbb}= Flat band voltage under back Gate

In case of subthreshold regime since the gate voltages are below the threshold voltage, the channel charge due to inversion layer is negligibly small and hence the inversion layer thickness may be neglected compared to the depletion layer depth.

The electric field due to the top and bottom gate of the proposed structures are shown in (2) and (3).

$$E_{Gate1} = \frac{V_{gbf} - V_{fbf} - \psi_{subSP}}{t_{ox}} \quad (2)$$

$$E_{Gate2} = \frac{V_{gbb} - V_{fbb} - \psi_s}{t_{ox}} \quad (3)$$

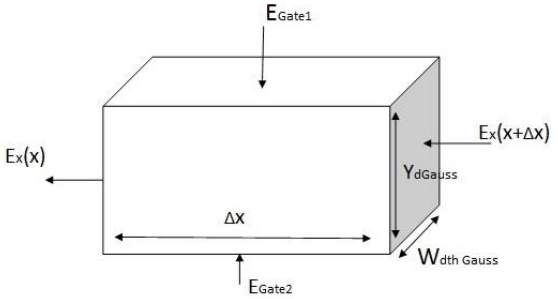

Fig 4: Rectangular Gaussian box covering the entire depletion layer depth is considered for the models

By ignoring the inversion layer charge in the weak inversion region, if we consider $n_{average\text{-}Gauss}$ as the substrate doping, then the total depletion charge due to the ionized acceptor atoms for the whole Gaussian surface considered, will be $-qn_{average\text{-}Gauss}\Delta x y_{dGauss} W_{dthGauss}$, where q is the electronic charge. If the dielectric permittivity of the medium is ε and the mobile charge carriers are ignored, after application of Gauss's law to the said surface, we get as in [3,4]:

$$\varepsilon \oint_{surface} \vec{E}.\overrightarrow{ds} = -qn_{average-Gauss} y_{dGauss} \Delta x W_{dthGauss} \quad (4)$$

By considering ε_{si} and ε_{ox} as the dielectric permittivity of the silicon and SiO_2 respectively, (4) will be expressed as follows:

$$-\varepsilon_{ox} E_{Gate1} \Delta x W_{dthGauss} + \varepsilon_{ox} E_{Gate2} \Delta x W_{dthGauss} + \varepsilon_{si}\{-E_x(x+\Delta x) + E_x(x)\} y_{dGauss} W_{dthGauss} = -qn_{average-Gauss} y_{dGauss} \Delta x W_{dthGauss} \quad (5)$$

By replacing $E_x = \left(\frac{d\psi_{SubSP}}{dx}\right)$ and solving (4) we get

$$-\varepsilon_{si}\left(\frac{d^2\psi_{SubSP}}{dx^2}\right) - \left(\frac{C_{ox}}{y_{dGauss}}\right)\psi_{SubSP} = qn_{average-Gauss} - \left(\frac{C_{ox}}{y_{dGauss}}\right)\left(V_{gsf} - V_{gsb}\right) \quad (6)$$

$$V'_{gsf} = V_{gsf} + V_{sb} - V_{fbf} \quad (7)$$

$$V'_{gsb} = V_{gsb} + V_{sb} - V_{fbb} \quad (8)$$

Where,

V_{gsf}/V_{gsf}= front/back gate to source voltage
V_{sb}=source bias voltage

V_{fbf}/V_{fbb}=front and back flat band voltage under the front and back gate of MOSFET.

For Single Metal Gate MOSFET
ϕ_M= work function of metal

$$\phi_t = \frac{kT}{q} \quad (9)$$

Where, ϕ_t= thermal voltage.

Halo Region Flat Band Voltage
For front gate:

$$V_{fbfp} = -\left(\frac{E_g}{2q}\right) - \phi_t \ln\frac{n_{average-Gauss}}{n_i} \quad (10)$$

For back gate:

$$V_{fbbp} = -\left(\frac{E_g}{2q}\right) - \phi_t \ln\frac{n_{average-Gauss}}{n_i} \quad (11)$$

Where,
$n_{average-Gauss}$= halo doping concentration
n_i= intrinsic carrier density
E_g=bang gap in silicon= 1.1eV
Fermi potential of n-type substrate

$$\phi_{fn} = \phi_t \ln\frac{n_{average-Gauss}}{n_i} \quad (12)$$

Where,
$n_{average-Gauss}$ = p-type substrate doping concentration
The flat band voltages for front and back gates are given in (13) and (14)
For front gate:

$$V_{fbf1} = (\phi_M - \phi_s)/q \quad (13)$$

For back gate:

$$V_{fbb1} = (\phi_M - \phi_s)/q \quad (14)$$

Since there is single material,

$$V_{fbf1} = V_{fbf2} \quad (15)$$

$$V_{fbb1} = V_{fbb2} \quad (16)$$

Work Function of Silicon Substrate

$$\phi_s = \left(\frac{E_g}{2q}\right) + \phi_{fn} + \chi \quad (17)$$

Where,
χ=electron affinity of silicon

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \quad (18)$$

Where,

C_{ox} stands for oxide capacitance per unit gate area
t_{ox} stands for gate oxide thickness
ε_{ox} stands for dielectric permittivity of SiO_2

$$y_{dGauss} = \sqrt{\frac{2\varepsilon_{si}\psi_{SubSP}}{qn_{average-Gauss}}} \quad (19)$$

Where,
y_{dGauss} stands for depletion layer depth under gate
ε_{si} stands for dielectric permittivity of Si

$$\text{And } \psi_{subSP} = \left(\frac{\gamma}{2} + \sqrt{\frac{\gamma^2}{4} + V_{gb} - V_{fb}}\right)^2 \quad (20)$$

Where,
ψ_{SubSP} stands for gate controlled sub threshold surface potential for long channel MOSFET

$$\text{And } \gamma = \frac{\sqrt{2q\varepsilon_{si}n_{average-Gauss}}}{C_{ox}} \quad (21)$$

Where γ stands for body effect coefficient
The depletion layer depth is non-uniform as a result of which, it is replaced by a polynomial of the following form:

$$y_{dGauss(x)} = (A_{Gauss}x + B_{Gauss})^2$$

Putting $y_{dGauss(x)} = (A_{Gauss}x + B_{Gauss})^2$ in (6) we get,

$$(A_{Gauss}x + B_{Gauss})^2 \frac{d^2\psi_{SubSP}}{dx^2} - \frac{C_{ox}}{\varepsilon_{si}}\psi_{SubSP} = \frac{qn_{average-Gauss}}{\varepsilon_{si}}(A_{Gauss}x + B_{Gauss})^2 - \frac{C_{ox}}{\varepsilon_{si}}(V_{gsf} - V_{gsb}) \quad (22)$$

The Channel Is Divided Into the Following Five Different Regions

Region 1

$$x_1 = 0 < x \leq x_2 = L_p(halolength)$$

$$y_1 = \left(X_{JGauss} + X_{RSGauss}\right) = (X_{JGauss} + \sqrt{\frac{2\varepsilon_{si}V_1}{qn_{average-Gauss}}})/\xi_s \quad (23)$$

Where,

$$X_{RSGauss} = \sqrt{\frac{2\varepsilon_{si}V_1}{qn_{average-Gauss}}} \quad (24)$$

ξ_s= fitting parameter for the source side takes into account the top and side fringing capacitances

$$\xi_s = \frac{4V_1}{V_{bi}} \quad (25)$$

$$y_2 = \frac{\sqrt{2\varepsilon_{si}\psi_{subSP1}}}{qn_{average-Gauss}} \quad (26)$$

Where,

$$\psi_{s1} = \left(-\frac{\gamma_p}{2} + \sqrt{\frac{\gamma_p{}^2}{2} + \left(V_{gbf} - V_{fbfp1}\right) - \left(V_{gbb} - V_{fbbp1}\right)}\right)^2 \quad (27)$$

$$\text{And} \quad \gamma_p = \frac{\sqrt{2q\varepsilon_{si}n_{average-Gauss}}}{C_{ox}} \quad (28)$$

Region 2

$$x_3 = x_2, x_4 = x_c$$

$$y_3 = y_2 = \sqrt{\frac{2\varepsilon_{si}\psi_{s1}}{qn_{average-Gauss}}} \quad (29)$$

$$y_4 = \sqrt{\frac{2\varepsilon_{si}\psi_{subSP2}}{qn_{average-Gauss}}} \quad (30)$$

Where,

$$\psi_{subSP2} = \left(-\frac{\gamma_p}{2} + \sqrt{\frac{\gamma_p{}^2}{2} + \left(V_{gbf} - V_{fbfp}\right) - \left(V_{gbb} - V_{fbbp}\right)}\right)^2 \quad (31)$$

Region 3

$$x_5 = x_4, \quad x_6 = L_1 x_7 = x_6, \quad x_8 = L - x_c$$

$$y_5 = y_4 = \sqrt{\frac{2\varepsilon_{si}\psi_{subSP2}}{qn_{average-Gauss}}} \quad (32)$$

$$y_6 = \sqrt{\frac{2\varepsilon_{si}\left((\psi_{subSP2}+\psi_{subSP3})/2\right)}{qn_{average-Gauss}}} \quad (33)$$

$$y_8 = y_6 = \sqrt{\frac{2\varepsilon_{si}\left((\psi_{subSP2}+\psi_{subSP3})/2\right)}{qn_{average-Gauss}}} \quad (34)$$

$$y_5 = y_7 = \sqrt{\frac{2\varepsilon_{si}\psi_{subSP2}}{qn_{average-Gauss}}} \quad (35)$$

Where,

$$\psi_{subSP3} = \left(-\frac{\gamma_a}{2} + \sqrt{\frac{\gamma_a{}^2}{2} + \left(V_{gbf} - V_{fbf1}\right) - \left(V_{gbb} - V_{fbb1}\right)}\right)^2 \quad (36)$$

And

$$\gamma_a = \frac{\sqrt{2q\varepsilon_{si}n_{average-Gauss}}}{C_{ox}} \quad (37)$$

Region 4

$$x_9 = x_8, \quad x_{10} = L - L_p$$

$$y_9 = y_8 = \sqrt{\frac{2\varepsilon_{si(}\psi_{subSP2}+\psi_{subSP3)}}{qn_{average-Gauss}}} \quad (38)$$

$$y_{10} = \sqrt{\frac{2\varepsilon_{si}\psi_{subSP4}}{qn_{average-Gauss}}} \quad (39)$$

Where,

$$\psi_{subSP4} = \left(-\frac{\gamma_p}{2} + \sqrt{\frac{\gamma_p{}^2}{2} + \left(V_{gbf} - V_{fbfp2}\right) - \left(V_{gbb} - V_{fbbp2}\right)} \right)^2 \quad (40)$$

Region 5

$$x_{11} = x_{10}, \qquad x_{12} = L$$
$$y_{11} = y_{10} = \sqrt{\frac{2\varepsilon_{si}\psi_{subSP4}}{qn_{average-Gauss}}} \quad (41)$$

$$y_{12} = \left(X_{JGauss} + X_{RDGauss}\right) = \left(X_{JGauss} + \sqrt{\frac{2\varepsilon_{si}V_7}{qn_{average-Gauss}}}\right)/\xi_d \quad (42)$$

Where,

$$\xi_d = \frac{4V_7}{V_{bi}} \quad (43)$$

And ξ_d= fitting parameter for drain side

The subthreshold surface potential for each of the five regions can be obtained as in [1,2,3,4]. From the expression of Subthreshold surface potential, the threshold voltage, which stands for the minimum gate to source voltage required for forming the inversion layer is obtained. Quasi-fermi potential based Drain current model is obtained considering the analytical value of Subthreshold surface potential as in [1,2,3,4].

3 SIMULATION RESULTS

The results obtained from the models are compared with those from DESSIS of ISE TCAD. In case of Dual Material Double Gate MOSFET, two Gate materials having different work functions are considered. The work function of first Gate material is considered greater than the work function of the second, such that, a step potential profile is formed in the channel region as a result of which, the Short Channel Effects are greatly suppressed in the proposed structures.

It is seen from Fig 5 that as the Drain to Source voltage is increased, the subthreshold surface potential since the value of potential is directly dependent on the applied Drain bias. It is also seen that at the channel length is reduced the Subthreshold surface potential minima shift upwards. The model result obtained for DHDMDG MOSFET with inner fringing field are compared with those from DESSIS. An appreciable agreement of the proposed model result from those from DESSIS are observed.

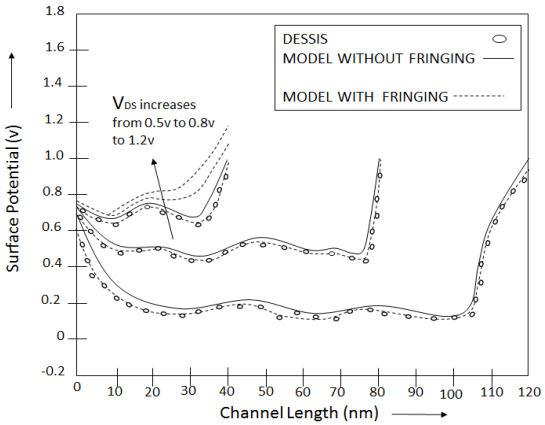

Fig 5: Comparative study of plots of Surface Potential vs Channel Length for DHDMDG MOSFET with and without Inner Fringing fields and variation of Subthreshold Surface potential for channel length=40 nm considering VDS=0.5,0.8 and 1.2V.

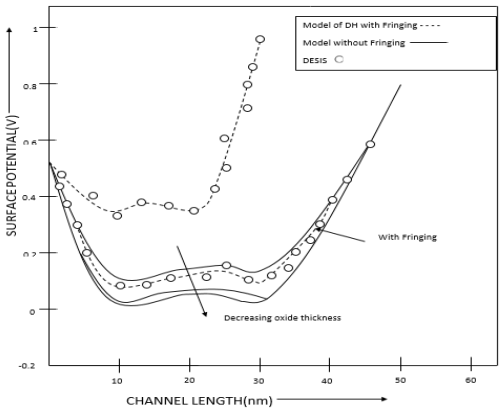

Fig 6: Comparative study of Subthreshold Surface potential vs Channel length for Double Halo MOSFET with and without inner fringing field and variation of Surface Potential with oxide thickness

Fig 6 shows that as the channel length is reduced the surface potential minima shift upwards similarly as in Fig 5. It is also found that as the oxide thickness is reduced the value of Subthreshold Surface Potential falls off. The model results with fringing capacitances are again compared with those from DESSIS.

From Fig 7 it is seen that the threshold voltage remains almost constant up to channel length 30 nm but falls off drastically after that. Due to the roll-off effect the proposed structure cannot be used for channel length below 30 nm. The threshold voltage is also obtained for three different values of Drain to Source voltage. It is seen that as a drain to source voltage is increased the roll-off effect decreases.

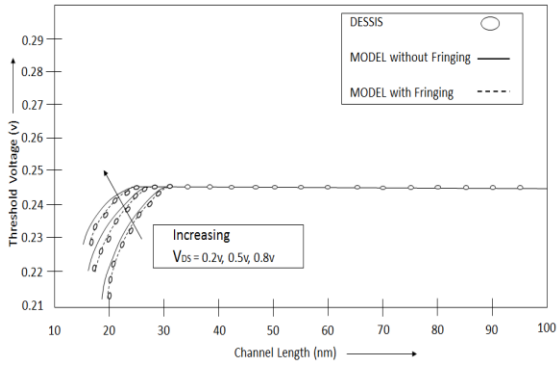

Fig 7: Plot of Threshold voltage vs Channel Length for channel length Gate Engineered Double Gate MOSFET with and without inner fringing field and variation of Threshold voltage with Drain bias

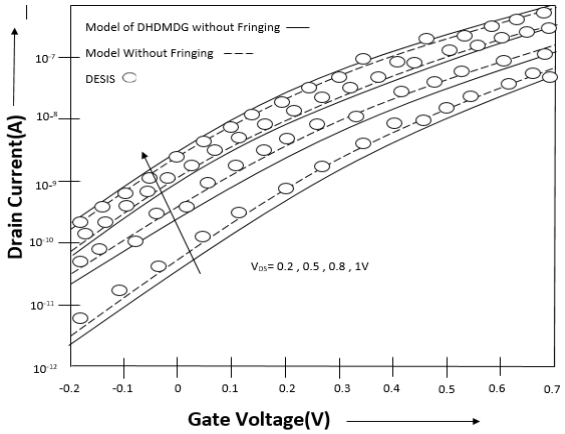

Fig 8: Comparative study of Drain Current with Gate to Source voltage for channel length Gate Engineered Double Gate MOSFET considering VDS=0.2,0.5,0.8 and 1V

It is seen that as the Drain to Source voltage is increased the subthreshold Drain current increases. This is Because with increase of drain bias the electric field from drain to source increases. As a result of which more electrons are drawn from the source to the drain end through the channel.

CONCLUSION

In this paper, an analytical expression of subthreshold surface potential, threshold voltage and drain current for Double Halo Dual Material Double Gate MOSFET is formulated, considering Gaussian halo doping concentration at the source and drain ends. Potentials due to inner Fringing Capacitances are also considered at the two ends. The results obtained are compared with those from DESSIS. It is concluded that Gaussian doped DHDMDG suppresses the short channel effects quite effectively upto a channel length of 30 nm, beyond which the threshold voltage roll-off degrades the device performance.

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