CORDIC Based Robot Navigation Processor Deploying RFID Technology

Subhashis Roy, Joyashree Bag, Subir Kumar Sarkar

Department of Electronics &Telecommunication Engineering, Jadavpur University, Kolkata-700032, India

subhashisaec@gmail.com, Joyashree.bag@yahoo.co.in, sksarkar@etce.jdvu.ac.in

Abstract: Efficient navigation in mobile robotics generally needs solving two important problems pertaining to the knowledge of the position of the robot and a motion control strategy. The problem becomes even more critical when no prior knowledge of the environment and surroundings is available where it is moving or in operation. These three independent tasks need to be solved in conjunction with the mobile robot navigation. Hence, a processor for the mobile robot navigation system has been proposed, designed, and implemented in the present work using Xilinx ISE14.3 simulation tools and Kintex7 FPGA board. Kintex™-7 FPGA board provides a wide-ranging, high-performance development with demonstration platform. The processor is efficient in avoiding collisions with mobile robots as well as with physical objects using RFID technology and a suitable algorithm. The use of RFID is justified because of RFID's computational simplicity compared to many of its counterparts in the state of the art. In order to improve the throughput and flexibility in the present processor implementation, CORDIC algorithm has been employed because of the simplicity of the operations incorporated in it, which make it very well suitable for VLSI implementation. Cadence design analyzer using 0.18μm CMOS technology shows that the throughput of this architecture is very high with a core area of 0.102 mm^2 only.

Keywords: Navigation processor; RFID technology; CORDIC algorithm; VHDL, FPGA.

1 INTRODUCTION

Intelligent robotic systems are extensively employed in different automation, defense and military services. Automation in hospitals, Mining and space exploration, office as well as smart laboratories are the most popular gift of intellectual robotic systems. In a mobile robotic system, other than motion control module, navigation is one of the most important modules. It also needs a prior information map about the travelling zone to avoid collision with other static

ISSN: 2222-7059 (print), ISSN: 2222-7067 (online), http://www.aspbs.com/aiem
DOI: 10.7508/aiem.2017.02.002

and dynamic objects. RFID i.e. radio frequency identification technology is a low power, faster wireless technology to identify a tagged object without line of sight. It is an emerging trend in modern electronic robotic system to incorporate the RFID technology to mitigate the collision problems and to enhance the performance of the robotic system. RFID technology has been employed in a multi-robot environment for many recently developed robot navigation techniques [1-3].

Advancement in VLSI technology has decreased the computational costs, hardware cost and computational power which trends the VLSI processors in modern communication devices. The processors based on reconfigurable high performance FPGA provide a better solution towards computing the position solution and navigation technique for robotic automation.

In view of the above it is found that there is still some scope to work in the area of robot navigation in order to avoid collision with a modified, low cost, high speed and efficient processor. Hence, in the present work, a power efficient mobile robot processor using COordinate Rotation DIgital Computer (CORDIC) algorithm has been modeled and realized up to RTL schematic level. The CORDIC algorithm provides a hardware efficient solution, reducing the gate count, computational complexity, thus hardware cost, thereby improving the processing speed and real time performance of the processor [4-6].

This paper also describes the basic CORDIC algorithm and its application for the implementation of the processor of a robot working with RFID technology. The Robot employs the processor to provide necessary control actions which is required by the robot in its dynamic condition. CORDIC algorithm has been applied for robot control, where CORDIC module serves as the functional unit of a programmable processor. Collision detection is another area where CORDIC has been applied to robotics. The collision detection problem is formulated as one that involves a number of coordinate transformations which are efficiently performed by CORDIC-based processing elements using only shift-add operations.

The rest of the paper is organized as: Section 2 describes the basic CORDIC algorithm; Section 3 introduces the proposed scheme with algorithm and experimental setup. The design of robot processor, test bench simulation results, synthesis report, and a comparative study with non-CORDICprocessor is given in Section 4 and finally we conclude with Section 5.

2 CORDIC ALGORITHM

CORDIC algorithm is used as a building block in different single chip solutions considering the critical aspects like low power, high speed, and small area to achieve reasonable overall performance. It is basically an iterative algorithm, requiring a simple shift and add operations, for hardware realization of basic elementary functions. J. E. Volder [4-5] implemented the basic CORDIC algorithm for multiplication, division, conversion of binary to decimal and mixed radix number systems and John Stephen Walther generalized the techniques proposed by J. E. Volder in order to compute hyperbolic, exponential, logarithm and square root functions [6-7]. CORDIC algorithm can be used to calculate different mathematical functions. CORDIC in rotation mode is described here to calculate the sine and cosine of an angle assuming the desired angle is given in radians and represented in a fixed point format.

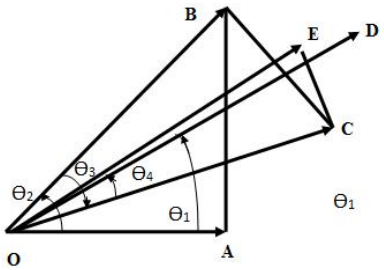

Fig. 1. Vector rotationfor CORDIC algorithm (A→B→C→E→……→D).

Successive iterations rotate the vector in one or the other direction by decreasing size steps so that the desired angle could be achieved. In Fig.1, the iteration steps are described clearly. Here, the desired angle is Θ1. In the first step, vector moves to angle Θ2 then angle Θ3 towards the desired angle Θ1 Every time it moves with decreasing step size and finally achieve the desired angle. So, after a sufficient number of iterations, the vector's angle will be close to the wanted angle Θ1. For most general purposes, 40 iterations (n = 40) are sufficient to obtain the correct result up to the 10th decimal place. The most important task left is to determine the direction of rotation, i.e. clockwise or counter-clockwise at each iteration and this is done by

determining the angle rotated at each iteration and subtracting that from the wanted angle. If it is negative, the rotation is counter-clockwise otherwise vice versa [7-9].

3 PROPOSED SCHEME AND EXPERIMENTAL SET UP

The aim of this work is to design the processor of the system combining the merits of VLSI design using RFID technology. The processor has been designed using RFID technology, which is fitted with the mobile robots and writable active tags with data frame structure as shown in Fig.2 and a reader.

Fig. 2. Entire data frame of the tag attached with the robot.

The reader continuously reads the tag ID which gets power from it. This data is transferred to the processor. The processor processes the data frame as per the design and the position coordinates are determined. The processor stores the tag ID and determines the distance of the tag from the reader and the zone ID. The zone with reference static tag indicates the zone ID of the robot. The processor measures the position coordinates (x1, y1) of the mobile robot with respect to the reference tag of that zone. Now, each robot will store its Zone ID, velocity and direction in its tag memory and will transmit this information to the other robots. Moreover, in its memory, it will store its instantaneous location coordinates and its destination coordinates [10].

An environment has been taken into consideration for four experimental case studies of the proposed system. Fig.3 shows the experimental set up depicting associated equipment and components required for the experiment.

a) Kintex™-7 FPGA board: The proposed robot processor design has been implemented using Xilinx ISE 14.3 simulation tools and verified its functionality using Kintex™-7 FPGA boards which provides a comprehensive, high-performance development and demonstration platform [11]. Kintex-7 FPGA board is a very high speed FPGA and used for new generation module for wireless communication system and very much suitable for portable module. It is highly integrated and has high speed connectivity with superior bandwidth. It has 8 Block RAMs configured within to build a 32 bit word memory. We have successfully downloaded the synthesized processor module on this board and verified its functional activity as the alternative controller board.

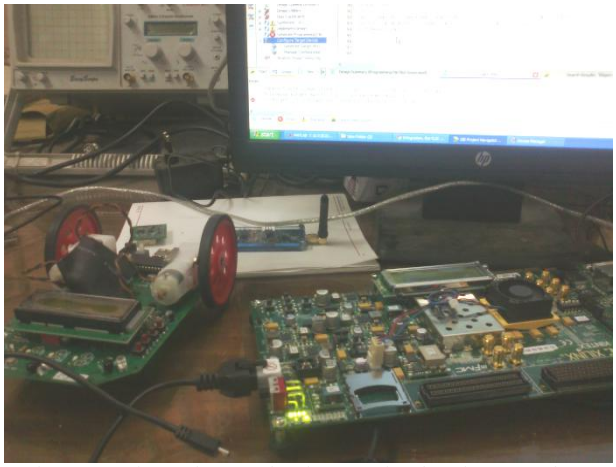

Fig. 3. Experimental set up showing associated equipment and components.

b) Active Reader and active tag: The Active reader is taken into account in order to determine the position of the mobile robot (attached with an active tag and unique tag ID) moving in a particular zone which is accessible by a control PC.

c) Passive Reader and passive tag: The passive reader is attached with each mobile robot in order to avoid collision using the proposed algorithm. To detect the static tagged object passive tags have been used. The RFID reader module is connected to the PC via a serial port and the baud rate of 9600 is fixed. The software for communicating with the reader is installed in the PC. When the tags come in contact with the range of a reader, the identity and type of tag are displayed on the PC screen.

d) FPGA compatible Mobile Robot platform: A mobile robot platform has been used for testing purpose where the controller processor is the FPGA. There is a provision to interface the FPGA with the robot to perform the desired control operation.

e) Xilinx ISE 14.3 simulation tools: The processor module has been simulated and synthesized in the Xilinx ISE environment. The suitable test bench simulation results are shown and the synthesis report has been included as tabular form in Table 1.

f) Control PC: The control PC detects the position of the robot wirelessly through active reader as well as their IDs. The software to detect the reader has been installed in the PC. The PC has i7-64bit processor, 8GB RAM with serial/USB/HDMI port connectivity.

g) Robotic platform: Qu-bot robot kit has been used for experimental purpose in the RFID environment using RFID reader and tags to verify the collision avoidance algorithm. It is very simple and user friendly for laboratory purpose.

Finally, according to our proposed and verified algorithm, we have developed the FPGA based processor to operate as the controller board of the robot.

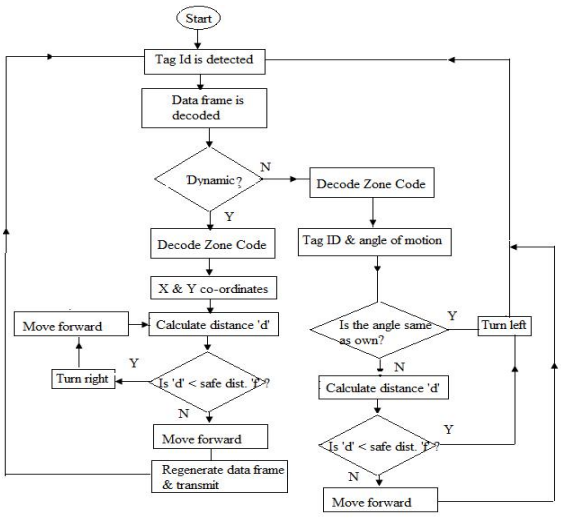

Fig. 4. Flow chart for operation of proposed system.

4 DESIGN AND SIMULATION OF ROBOT PROCESSOR CIRCUIT

Where CORDIC block generates the Sine and Cosine functions which in turn modifies the processor. To enhance the processor speed, the other multipliers also replaced by CORDIC block and these blocks have been incorporated in the Final processor module of the robot. The VHDL code is simulated in Xilinx 14.3 ISE with appropriate input signals for each operational block. All the operational blocks are then incorporated into a single processor and simulated. After the successful synthesis of the processor design, we achieve the RTL schematic view and HDL synthesis report as well as the device utilization chart of the processor. The RTL representations and technology views of the proposed system is needed for the proposed hardware design. The operational flowchart is given in Fig. 4.

There are two major blocks in the system. The 'Data Frame Generator block' generates the position co-ordinates (x, y), calculates its Zone ID, velocity &angle of motion and generates the 46-bit data frame to be transmitted. This unit incorporates the CORDIC block in order to calculate these parameters consist of angles and several multiplications. The second block is the 'Decision Block' which performs the task of controlling the decision of Robot regarding its route of motion. The Test bench simulation results of the Data Frame Generator and Decision block are shown in Fig.5 and Fig.6 respectively.

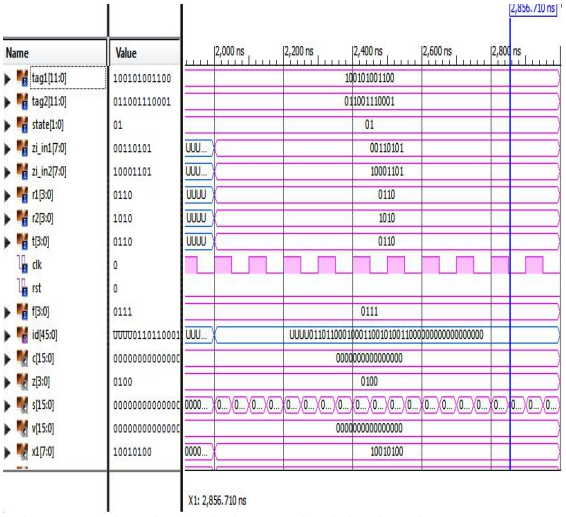

Fig. 5. Test bench simulation result of the data frame generator.

Fig.5 shows the test bench simulation result of the Data Frame Generator. Now the Data frame is generated and transmitted by the robot as well as it stores the data in memory. It is further used by the second part of the processor for taking decision to 'move forward' or 'turn left/right' and detect other tags in order to move in a collision free environment by continuously tracking the distance of other objects.

In the second part the Decision module, there is an input terminal which detects the data frame transmitted by other robots. It identifies the zone ID, tag ID, and other relevant information of the detected tag of other robot after it decodes the data frame. Now, it takes appropriate decision to avoid collision with other static/dynamic objects/robots maintaining a safe distance 'f'. Two output terminals 'L' and 'M' are considered for this purpose. In the output port,

when 'L' is high ('1') and 'M' is low('0'), the robot turns left and try to detect other tags and vice versa.

In Fig.6 we observe that situation where the distance between two robots is equal to the safe distance 'f' and 'L' is high, indicating the robot to turn left.

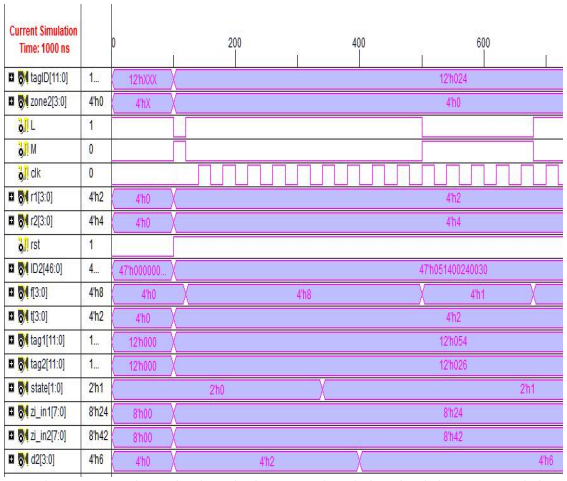

Fig. 6. Test bench simulation result of the decision part of the processor.

The synthesis report obtained from successful synthesis of processor design module using Xilinx ISE 14.3 simulation tools, and implementation on reconfigurable Kintex-7 FPGA kit for real time verification. New generation of module with embedded FPGAs are being constructed to provide system level enhanced performance [11, 12]. The process of detection and checking is perpetual. The other cases of checking are alsocarried out and its result is in agreement with the expected one thereby establishing the suitability of our processor. The advanced synthesis report and device utilization chart for our implemented processor shows improvement over non CORDIC based robot processor [13] in terms of required multipliers, maximum combinational path delay and dynamic power dissipation. The area utilization is solely based on logic utilization in case of an FPGA. Hence, little information we get regarding die area and the distribution of transistors for logic or routing. Hence, the cell architecture has been implemented using CADENCE design suit for placement and routing to get idea of area requirement for the proposed single chip processor. Instead of building one universal fabric for all designs, we built a customized fabric for each design. The layers of routing are allowed to be modified with design requirements and algorithms. The worst case timing libraries are used during place & route. Cadence design analyzer shows that the throughput of this architecture is high with core area of 0.102 mm^2.

CONCLUSION

A powerful efficient robot processor has been realized in this paper using VHDL coding and Xilinx ISE 14.3 simulator. In order to substantiate real time verification of the processor high performance FPGA Kintex-7 is used here. The synthesized result of 32-bit word size processor architecture with commercially available 0.18 μm CMOS technology using Cadence design analyzer shows that the throughput of this architecture is high with core area of 0.102 mm^2. It is further observed that the overall power dissipation has reduced due to use of CORDIC algorithm.

ACKNOWLEDGMENT

The authors thankfully acknowledge the support of UGC sponsored UPE phase II project of Jadavpur University, Kolkata, India.

REFERENCES

[1] O. Khubitz, R. D. Matthias and O. Berger, 2002. Application of radio frequency identification devices to support navigation of autonomous mobile robots, IEEE Vehicular Technology Conference, pp. 256-264,

[2] H. Chae and K. Khan, December 2005. Combination of RFID and vision for mobile robot localization, Intelligent Sensors,Sensor Networks and Information Processing Conference, Munich, Germany, pp. 75-80.

[3] T. Tsukiyama, 2005. Global navigation system with RFID tags, Proceedings of SPIE, vol. 6006, pp. 412-419.

[4] J. E. Volder, Sept. 1959. The CORDIC trigonometric computing technique, IRE Trans. Electron. Computers, vol. EC-8, pp. 330-334.

[5] J. E. Volder, 2000. The birth of CORDIC, J. VLSI Signal Process., vol. 25. pp. 101-105.

[6] J. Bag, S. Roy, P. K. Dutta, and S. K. Sarkar, 2014. Design of a DPSK Modem Using CORDIC Algorithm and Its FPGA Implementation", IETE Journal of Research. vol. 60, no. 5, pp. 355-363.

[7] J. S. Walther, 2000. The story of unified CORDIC, J. VLSI Signal Process., vol. 25, no. 2, pp. 107-112.

[8] Y. H. Hu and S. Naganathan, 1990. A Novel implementation of chirp Z-transform using a CORDIC processor, IEEE Trans. Acoust, Speech, Signal Process. vol. 38, no. 2, pp. 352-354.

[9] Y. H. Hu. 1992. CORDIC based VLSI Architectures for Digital Signal Processing', IEEE Signal Processing Magazine, pp.16-35.

[10] D. Perry, 2002. VHDL: Programming By Example.

[11] V. A. Pedroni, 2010. Circuit Design and Simulation with VHDL .

[12] P. J. Ashenden, 2008. The Designer's Guide to VHDL.

[13] J. Bag, K. M. Rajanna and S. K. Sarkar, 2012. Design and VLSI Implementation of Anti - collision Enabled Robot Processor using RFID technology, Int. Journal of VLSI design & Communication Systems (VLSICS). vol. 3, no.6, pp 51 -65.