Design of 4 Bit Rotate Left Network at Low Power and Small Delay Using MOS Transistor at 45 nm Channel Length

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Abstract: In this work the design of 4 bit rotate left network with Metal Oxide Semiconductor (MOS) transistor having channel of 45nm has been presented. To report average power consumption and delay of the network the magnitude of the voltage of control signals and signal sources has been diverse from 0.5 V to 1.2 V .The measured value of average power consumption is 19μW and gate delay is 17.3ps at on voltage of 1 volt. The overall circuit has been simulated using Tanner SPICE (T-SPICE) software.

Keywords: rotate left, nano, power, delay, T-SPICE

1 INTRODUCTION

For arithmetical and logical operation rotate left shift network has wide application [1, 2]. The design of 4 bit rotate left network has been presented in this work. Now days the design of very large scale integrated (VLSI) circuit at low power consumption is a major issue [3]. Switching power, short circuit power, leakage powers are the main sources of power consumptions in VLSI circuit [4]. Dynamic or switching power consumption is principal source of power consumption among these [5]. For miniaturization as circuit dimensions are shrinking down leakage power consumption of the circuit has been increased [6]. Therefore design with nano dimension MOS transistor for low power application is the challenges to the VLSI designer without lacking the performance of the circuit [7]. Gate delay is also one of the design metric contexts to speed of the circuit [8-9]. In this work delay analysis and average power consumption analysis of 4 bit rotate left network has been performed varying the on voltage of the input signal and control signal [10].

2 DESIGN AND SIMULATION OF 4 BIT ROTATE LEFT NETWORK

The circuit diagram of rotate left network is shown in Fig. 1. The structure looks like a 4×4 array structure. al0, al1, al2, al3 are the nodes of four

ISSN: 2222-7059 (print), ISSN: 2222-7067 (online), http://www.aspbs.com/aiem
DOI: 10.7508/aiem.2017.02.012

input signal sources. Similarly rol1, rol2, rol3 and rol4 are the nodes for control signal source. rol1, rol2, rol3 and rol4 are used as control signal for rotating bit pattern towards left. Outputs of the network are investigated at terminals yl0, yl1, yl2 and yl3. Rotating operation logic for the design is

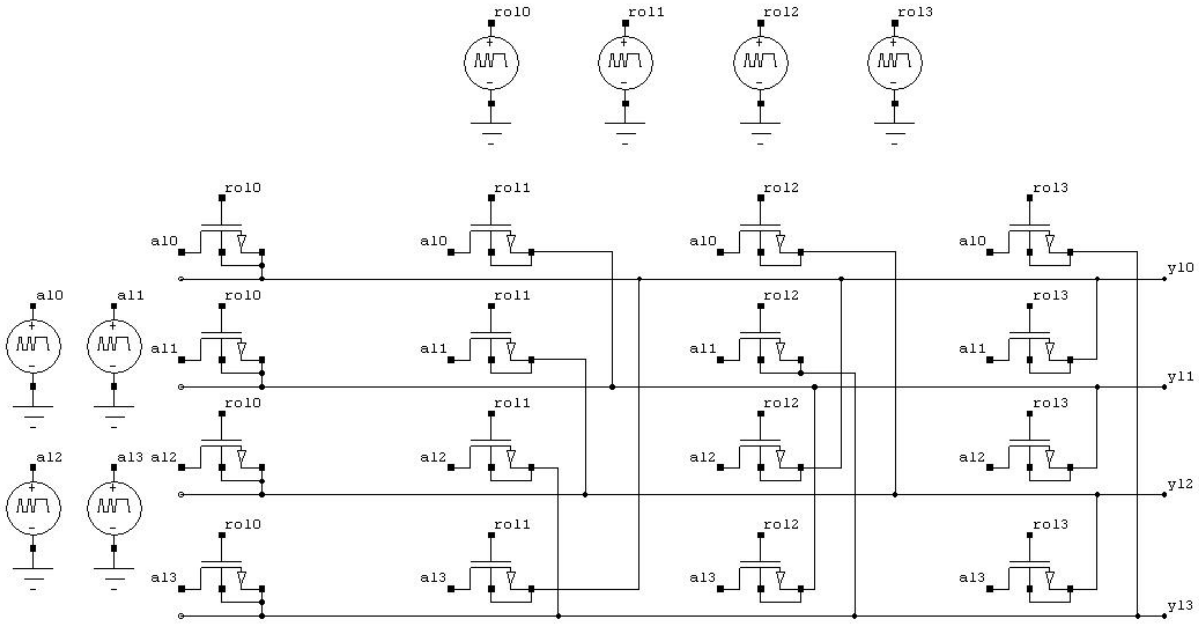

Fig. 1. Circuit Diagram of 4 bit rorate left network.

Table 1. Logic for Rotating Bit in Left Wards Direction.

Condition of Control Signal				Output			
rol0	rol1	rol2	rol3	yl3	yl2	yl1	yl0
1	0	0	0	al3	al2	al1	al0
0	1	0	0	al2	al1	al0	al3
0	0	1	0	al1	al0	al3	al2
0	0	0	1	al0	al3	al2	al1
1	0	0	0	al3	al2	al1	al0

in Table 1. Out of four control signal only one control signal is maintained at logic high at a time. From the Table 1 it has been observed that if control signal rol0 is at logic high output is yl3yl2yl1yl0=al3al2al1al0. For the following next rotation whenever rol1 is at logic high, output becomes yl3yl2yl1yl0=al2al1al0al3. This indicates that the output pattern has been rotated left by one bit position. In this way the positions of the bits are shifted as shown in Table 1 for consecutive rotation. The circuit of 4 bit rotate left network has been configured and simulated using MOS transistor at channel length of 45nm. The channel width (W) to channel length (L) of all the NMOS in the circuit has been taken as 3:1 ratio. The functionality of the circuit has been verified with help of T-SPICE tools. The input and output waveforms are shown in Fig.2 and Fig.3 respectively.

Fig. 2 and Fig. 3 show the rightness of the design.

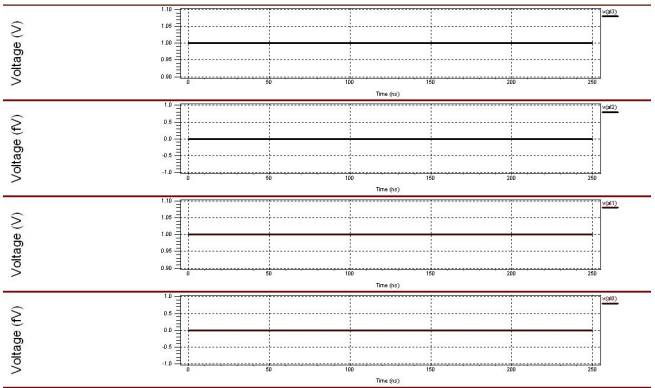

Fig. 2. Input signal al0, al1, al2, al3.

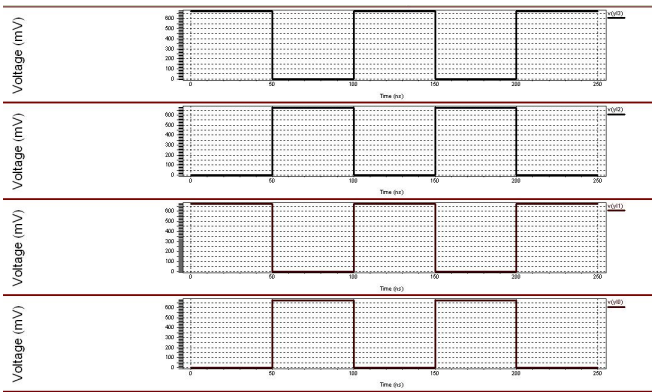

Fig. 3. output wave forms yl3, yl2, yl1, yl0.

3 AVERAGE POWER CONSUMPTION ANALYSIS OF 4 BIT ROTATE LEFT NETWORK

The average consumption across the 4 bit rotate left network has been measured at 45nm channel length of MOS transistor. To observe the variation of power consumption, on voltage of the signal sources has been varied from 0.5 V to 1.2 V. The results are depicted in Table 2. The graphical representation of power consumption is shown in Fig.4.

Table 2. Average power consumption (WATT) across 4 bit rotate left network at 45nm channel length of MOS transistor.

On Voltage of Input Signal Source (Volt)	Average Power Consumption Across 4 Bit Rotate Left Network (Watt)
0.5	4.99E-08
0.6	9.79E-08
0.7	3.21E-07
0.8	1.33E-06
0.9	5.44E-06
1	1.90E-05
1.1	5.06E-05
1.2	1.03E-04

Table 3. Input to output gate delay at channel length of 45nm.

On Voltage of Control Signal (Volt)	Delay (Sec)
0.5	6.39E-11
0.6	3.28E-11
0.7	3.06E-11
0.8	2.41E-11
0.9	1.99E-11
1	1.73E-11
1.1	1.55E-11
1.2	1.38E-11

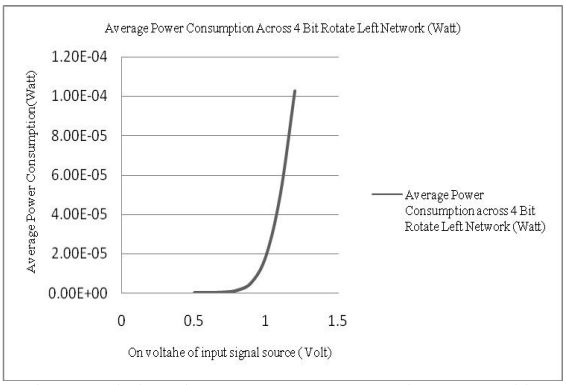

Fig. 4. Variation of average power consumption across 4 bit rotate left network.

It has been observed from Table 2 and also Fig. 4 that as on voltage decreasing power consumption across the circuit also decreasing. Average power consumption across the circuit is 19 μW at on voltage of 1V .

4 DELAY ANALYSIS OF 4 BIT ROTATE LEFT NETWORK

Speed of operation of circuit depends on the gate delay. The variation of the gate delay has been observed by changing the magnitude of on voltage of the control signal. The results are represented in Table 3. The graphical representation of results from Table 3 is shown in Fig.5. From the simulation results the delay across the circuit is 17.3 ps at on voltage of 1 V. The result are satisfactory for high speed VLSI circuit.

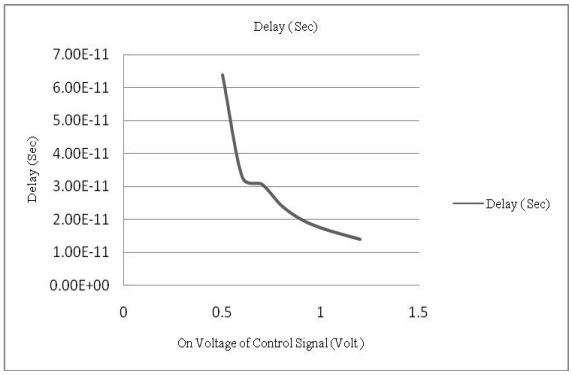

Fig. 5. Variation of delay vs. on voltage of control source.

5 CONCLUSION

The 4 bit rotate left network has been designed successfully in this work. The average power consumption and gate delay across the network has been reported and analyzed varying the magnitude of on voltage of the input signal source and control signal source from 0.5 V to 1.2 V. The measured value of average power consumption and gate delay are satisfactory context to low power and high speed VLSI circuit design. It also seen that due to decreasing on voltage the average power consumption across the circuit decreases however delay of the circuit increases. So for enhanced performance of the circuit, optimization of power and delay with respect to the on voltage is the scope of the future work.

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