7-Segment Decoder in Near Threshold Regime for Ultra Low Power Application

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Abstract: Energy and power are the two most primary design parameters. Over the last few decades, we observed a steady increase in the count of transistors on a chip conforming Moore's law leading to advancement in various computing accomplishments. But the largest hindrance to this flourishing growth is related to energy and power consumption and thus finding energy-efficient solutions is very much crucial for the sustenance of the semiconductor industry. Therefore, the aim of the designers in this era is to overcome the challenge of energy efficient computing and make performances free from the realms of power through voltage scaling techniques. Till now voltage scaling techniques have proved to be very effective but with subthreshold design representing the ultimatum of voltage scaling. However, subthreshold design has certain major performance penalties. This paper defines and explores design space called the near-threshold region. This region retains much of the energy savings of subthreshold operation with more favorable performance and variability characteristics.
Keywords: Near-threshold; 7-segment display; CMOS.

1 INTRODUCTION

Energy efficiency has now become the primary obstacle in scaling the performance of all classes of computing systems. Low-voltage computations, specifically near-threshold voltage computing (NTC), which involves operating the transistor very close to and yet above its threshold voltage, holds the promise of providing many-fold advantages and improvements in terms of energy efficiency. The utilization of ultra low-voltage operation, subthreshold operation ($V_{dd} \sim V_{th}$) to be more specific, was first proposed around three decades ago when the theoretical lower limit of Vdd was found to be around 35 mV. But because of some obstacles and performance penalties subthreshold operation is confined to a handful of products such as hearing aids and wristwatches. Thus, to the designers, working in this region has remained nothing more than a fascinating concept with no practical importance. Considering the current energy crisis in the semiconductor industry and constant voltage scaling we understand the necessity for a complete shift where ultralow-power operation is applied across application platforms and forms the basis for renewed energy efficiency. But NTC does not come without some drawbacks to its widespread acceptance. Some of these barriers include loss in performance, increase

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in performance variation, and increase in functional failure rate of memory as well as increased logic failures and overcoming these barriers is itself a big challenge.

Energy consumption in recent CMOS circuits mostly occurs from the charging and discharging of internal capacitances and can be reduced considerably by changing the voltage (Vdd) supply. Scaling the supply voltage has proved to be one of the most fruitful methods to reduce power consumption in commercial applications. It has been seen that CMOS circuits function well at very low voltages and remain functional even further when Vdd goes below the threshold voltage (Vth). For a long time, there has been extensive research in subthreshold operation, primarily for analog circuits and of late for digital processors featuring near Vdd below 200 mV. Now, it is extremely vital to obtain the exact Vdd at which the energy is maximum. In the super threshold regime (Vdd > Vth), energy is very much sensitive to Vdd, performance is very high with huge consumption in energy. Hence voltage scaling down to the near-threshold regime (Vdd ~ Vth) yields an energy reduction on the order of 10X at the cost of approximately 10X performance degradation. [1] However, the dependence of energy on Vdd becomes more difficult to explain as voltage drops down below Vth. In subthreshold (Vdd < Vth), delay in the circuit usually increases exponentially with Vdd, causing leakage energy (the combined result of leakage current, Vdd, and delay) to increase in a near-exponential manner. This rise in leakage energy eventually dominates over switching energy, resulting in an energy minimum. The identification of an energy minimum is the next step to find the processors that operate at this energy optimal supply voltage (referred to as V_{min} and typically 250 mV–350 mV). Energy typically reduces by only 2X when Vdd is scaled from the near-threshold regime (400–500 mV) to the subthreshold regime, but simultaneously the delay rises by 50–100X over the same region. Although it is acceptable in ultralow energy based systems, this delay penalty is not acceptable for broader application categories. Hence, although introduced roughly 30 years ago, ultralow-voltage design remains confined to a small set of markets with little or no impact on mainstream semiconductor products [2].

The opportunities in this design space include the new architecture, optimization of processes and the less thermal restrictions. On the contrary there are also some challenges associated with working in this domain like performance loss, sensitive to variations in threshold voltage, increased probability of timing errors, and expensive error recovery mechanisms. One of the major pitfalls of this near threshold computing is the 10X performance loss. To enable extensive universal application of NTC this 10X performance loss must be succeeded while conserving the energy efficiency. To recover the performance loss in NTC without increasing supply voltage, Zhai et al. proposed the use of NTC-based parallelism. In applications where there is plenty of thread-level parallelism the objective is to use 10 s to 100 s of NTC processor cores that will regain 10–50X of the performance, while remaining energy efficient [3].

2 BASIC OPERATION OF 7-SEGMENT DISPLAY

A seven-segment display is a form of electronic display for displaying decimal, alphabets and numerals. Normally seven segment display letters from a-g and numbers from 0-9. It is composed of seven elements, made with LED's. Numbers like 0-9 can be displayed and some of the alphabets that can be possible in seven-segment by turning different LED's on or off individually. Seven – segment decoders are used to take a four-bit BCD input and provide the outputs that will pass current through the appropriate segments to display the corresponding appropriate decimal digit. It can be basically operated in two modes - the common cathode and common anode. In common Anode display, the anode of all the LED's on the segment are collected and joined together and the individual segments are illuminated by connecting to a Low voltage whereas in a common cathode display, the cathodes of the LED's are joined together and the individual segments are illuminated by connecting to high voltage [5, 6].

In this paper, we have tried to implement the 7-segment decoder driver in near threshold and analyze its performance so that it can be used in some low power display device applications.

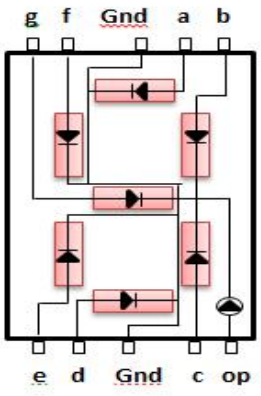

Fig. 1. Diode connections.

Table 1. Truth table of 7-segment display.

Digit	A	B	C	D	A	B	C	D	E	F	G
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

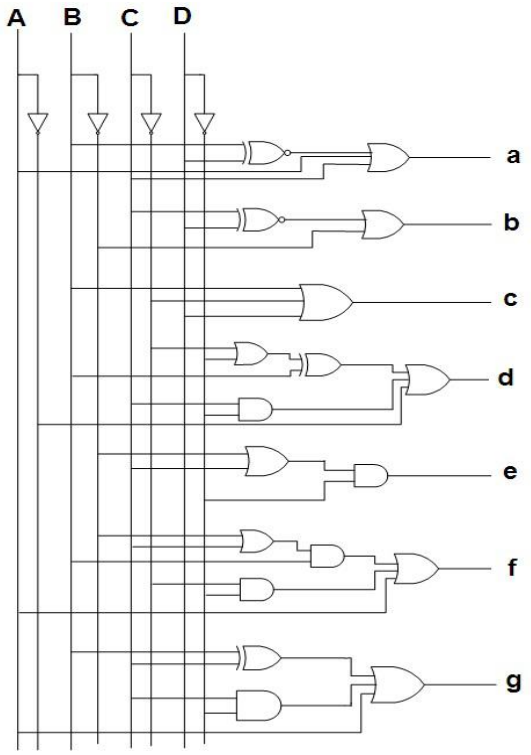

Fig. 2. Schematic of 7-segment display.

The Boolean Expressions of a, b, c, d, e, f, g, are as follows:

i. $a = A + C + BD + \overline{B}\overline{D}$

ii. $b = \bar{B} + \overline{C}\overline{D} + CD$

iii. $c = B + \bar{C} + D$

iv. $d = \overline{B}\overline{D} + \overline{C}\overline{D} + B\bar{C}D + \bar{B}C + A$

v. $e = \overline{B}\overline{D} + C\overline{D}$

vi. $f = A + \overline{C}\overline{D} + B\bar{C} + B\overline{D}$

vii. $g = A + B\bar{C} + \bar{B}C + C\overline{D}$

3 PROPOSED STRUCTURES IN NEAR-THRESHOLD REGIME

We have simulated the codes of the 7 LED's namely 'a', 'b', 'c', 'd', 'e', 'f' and 'g' (circuits shown below) using the concept of sub-circuits in Tanner Spice Software using 22nm technology and obtained the average power and voltage swing characteristics of the 7-segment driver by varying the supply voltage (Vdd), temperature and load in the near threshold regime. Here the supply voltage is approximated to be around 350 mV. Extensive simulations have been made by varying supply voltage from 300 mV to 500 mV, temperature has been varied from -30 degree to around 120 degree centigrade and load from 10 femto farad to 50 femto farad. Our proposed strategy is to provide 10X or higher energy efficiency improvements at around 10X performance degradation through widespread application of Near-Threshold Computing (NTC), where devices are operated at or near their threshold voltage (Vth). By reducing supply voltage from a nominal 1V to 400–500 mV, NTC obtains as much as 10X energy efficiency gains and represents the reestablishment of voltage scaling.

Following shows the CMOS implementations of the Boolean expressions mentioned above.

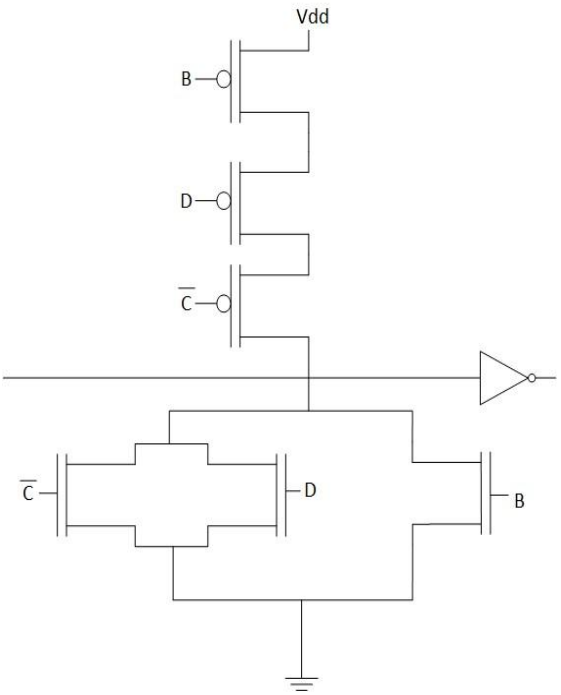

Fig. 3. 'a'

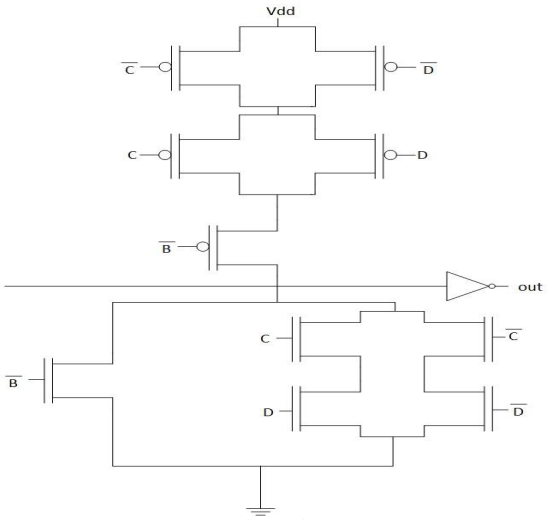

Fig. 4. 'b'

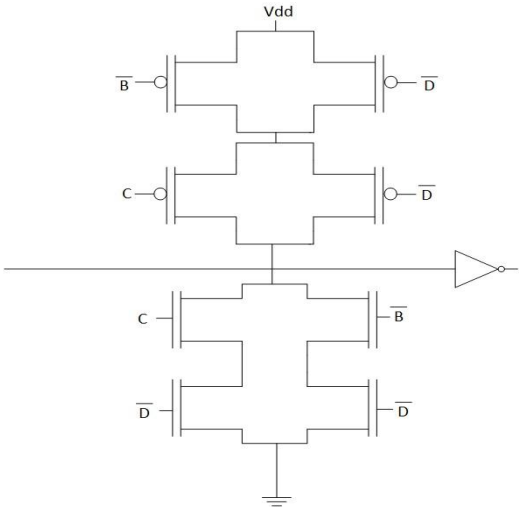

Fig. 7. 'e'

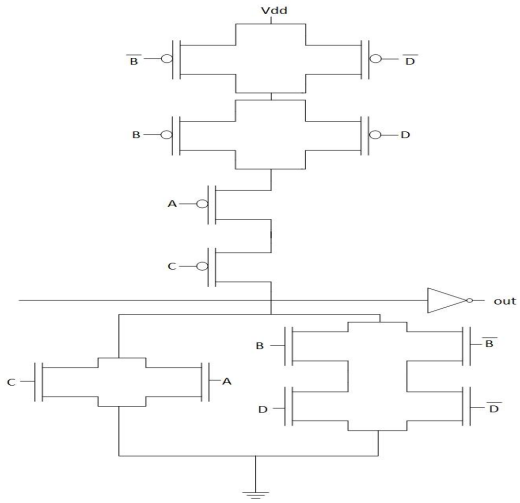

Fig. 5. 'c'

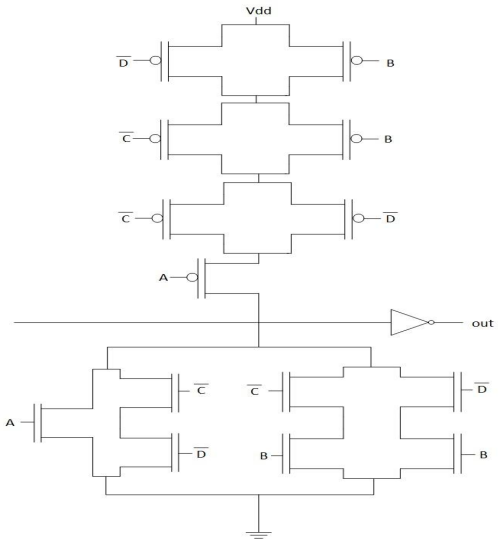

Fig. 8. 'f'

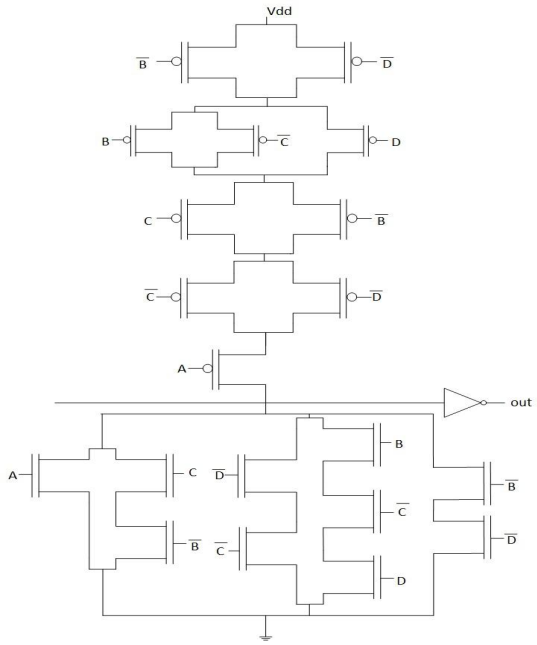

Fig. 6. 'd'

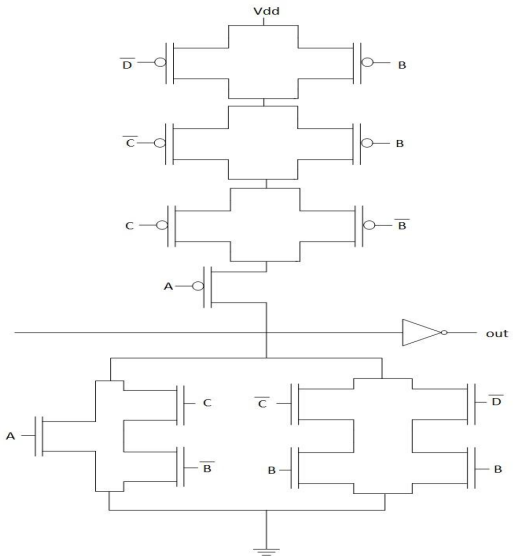

Fig. 9. 'g'

4 RESULTS AND SIMULATIONS

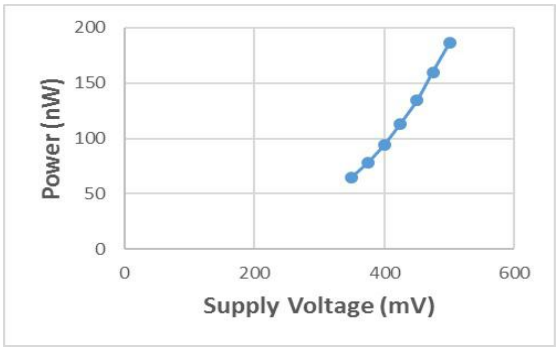

Fig. 10. Variation of power (nW) with supply voltage.

In Fig. 10, we observe that power increases with the supply voltage. At around 350 mV supply the power is found to be 65 nW and at 500mV the power observed is 164.8 nW. So although power increases, it is quite insignificant compared to super threshold.

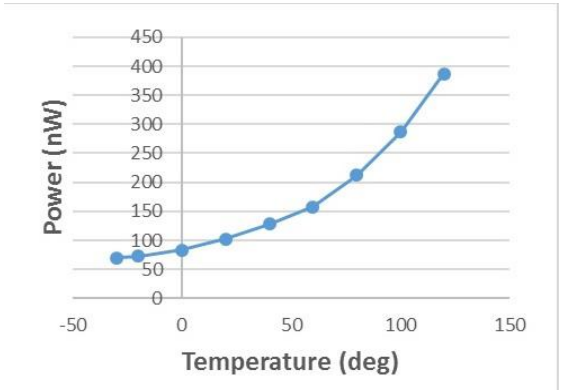

Fig. 11. Variation of power (nW) with temperature.

Here from Fig. 11, we find that the minimum power at -30 degree centigrade is approximately 69.8 nW and at 500 mV the power observed is 387.414 nW. There is an increase in power with the increase in temperature.

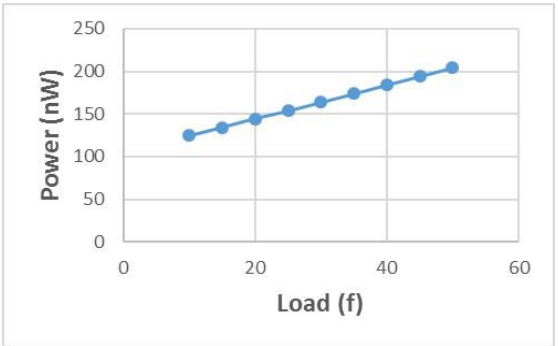

Fig. 12. Variation of power (nW) with capacitive load (fF).

In Fig. 12, we observe that power increases linearly with the capacitive load. At 10 fF the simulated power is 129 nW and at 50 fF the power is 204 nW.

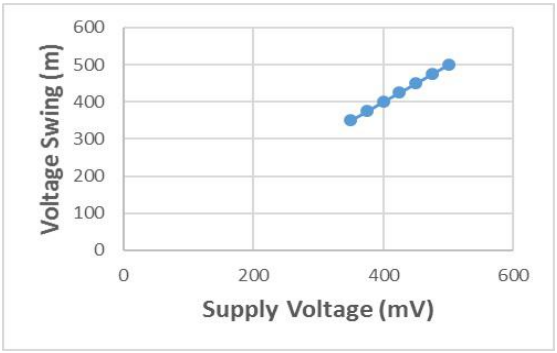

Fig. 13. Variation of voltage swing (m) with supply voltage.

In Fig. 13, we observe the voltage swing characteristics against supply voltage. Here also a linear pattern is observed, the minimum swing at 350 mV is found to be 349 mV and the same at 500 mV is found to be around 449.5 mV

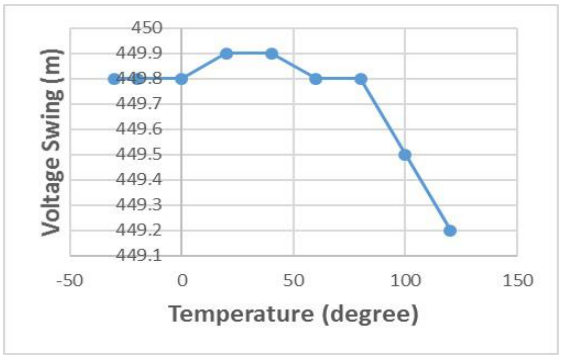

Fig. 14. Variation of voltage swing (m) with temperature.

In Fig. 14, although we observe there is no linear relationship between voltage swing and temperature. Apparently, it seems that voltage swing varies abruptly without any particular pattern but if we observe minutely we find that the swing varies between 449.1 mV and 449.9 mV which is considered to be quite insignificant.

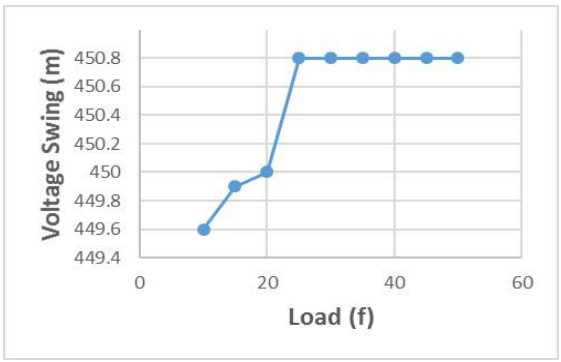

Fig. 15. Variation of voltage swing (m) with load.

In Fig. 15, we observe the voltage swing increases with the capacitive load up to a certain point (25 fF) and then it attains saturation.

So overall, improvement in swing and deterioration of power have been observed in the graphs plotted

above. Although an increment in power is noted when the latter is varied with each of supply voltage, temperature and load but it is much less when compared with super threshold. Voltage swing is observed to be almost constant in each of the cases. Therefore, to summarize in super threshold performance is very high, huge amount of current can be driven but at the same time there is huge power consumption whereas in sub threshold although energy consumption decreases by some factor with performance decreasing exponentially but delay increases in the circuit by many folds. But in near threshold operation even though there are some performance degradation still it can drive a moderate amount of current and at the same time power is moderately less. Thus, we can say that in systems where speed is not an issue near threshold operation can be well considered as a compromise between the two. Nowadays it has been widely used in many low power applications like the tachometer, smart watches, smart phones, digital thermometer, blood glucose monitor and many other biomedical instruments.

5 CONCLUSION

In conclusion, we can say that although Moore's law always keeps providing engineers with increasing number of transistors on a fabricated integrated chip but power budgets are captivating the applicability of these additional transistors in conventional CMOS design. In this paper, we laid emphasis on the feasibility of voltage scaling to reduce energy consumption. Although subthreshold operation is well known to provide energy savings of considerable importance it can be used to a handful of applications due to the corresponding degradation in performance. Thus, we turned to the concept of near-threshold computing (NTC), and tried implementing the 7-segment display driver in the near-threshold regime which enables energy savings on the order of 10X, with only a 10X degradation in performance, providing much better energy-performance characteristics than subthreshold operation.

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