Design of High Speed, Area Optimized and Low Power Arithmetic and Logic Unit

S. Swetha[1*], MD. Afreen Begum[2]

Department of ECE, CVR College of Engineering, Ibrahimpatnam-501510, India

[1]swetha.sillveri@gmail.com

[2]afreeen208@gmail.com

Abstract: Optimization of area, delay and power dissipation is the major issue in low voltage and low power applications. GDI-Gate Diffusion Technology is low power digital combinational design. This technology requires less number of transistors compared to conventional CMOS technology. As the number of transistors reduced, then optimization of area and power is achieved. One of the disadvantages of GDI is poor logic swing, which is overcome by modifying this technique. This paper mainly presents the optimized area and low power 8-bit ALU using Modified Gate Diffusion Input Technique. This technique allows a reduction in area, delay and low power dissipation with full logic swing. Full adder is a basic cell in ALU which is designed using XOR-MUX to have an operation with high-speed and low power. The entire design is done using CADENCE Tool in GPDK 90nm and 45nm technology. Power and delay comparison between conventional CMOS, GDI and Modified GDI is also presented.

Keywords: GDI; modified GDI; CMOS; full wing; ALU; low power; MUX; ALU.

1 INTRODUCTION

Due to the evolution of nanotechnology, the low power and high speed microelectronic devices has come to the forefront. Now a day there is a rapid increase in the use of portable applications, it demands small-size, low power, high speed and high throughput circuitry. To improve the performance the performance of circuits based on CMOS logic many logic styles are introduced like Pass transistor logic (PTL), Domino logic, Transmission Gate logic, Double pass transistor logic (DPTL) etc. Gate Diffusion Input (GDI) is a new method for low power digital combinational circuit design [2]. The basic cell consists of two transistors, with three input terminals Gate, P-diffusion and N-diffusion [2].Advantage of GDI is low power, delay and area. But the disadvantage of GDI is output doesn't have full swing logic

This paper proposes a low power, high speed and area optimized 8-bit ALU using Modified GDI multiplexer with full swing logic. A Multiplexer and Full adder are the major blocks in ALU design. In this one-bit Full Adder is also designed Modified GDI multiplexer to achieve full swing logic, low power dissipation and less delay. Total work is done using CADENC Virtuoso Tool.

2 ARITHMETIC AND LOGIC UNIT

An Arithmetic and Logic Unit (ALU) is a digital circuit which performs arithmetic and logical functions. ALU is a fundamental and major block in central processing unit of a computer which performs computer's data processing functions. Based on the ALU design the computational efficiency of a computer is determined as the modern CPU's and graphical processing units

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(GPU) accommodate very powerful and complex ALU's [4].

The proposed ALU is designed using Modified GDI Multiplexer [6]. For optimizing area and power design is done using 4X1 Multiplexers.1-bit full-adder is implemented with 6Tr XOR and 6Tr Multiplexer to achieve full swing in the output. All arithmetic and logical operations like addition, subtraction, increment, decrement AND, OR, XOR, NOT, logical shift operations are carried out inside the ALU.

3 EXISTING SYSTEM

In existing methods ALU consists of 4x1mux, 2x1mux and full-adders which implements seven arithmetic operations and four logical operations [3]. In proposed method full adder is implemented using 6Tr 2x1MUX using Modified GDI technique, to achieve high speed and low power. Along with the above said operations, ALU also performs logical shift left, shift right, rotate left and rotate right operations.

3.1 Design of Full Adder

Full adder is a combinational circuit that performs arithmetic sum of three bits. It consists of three inputs and two outputs-sum and carry. Logic diagram of full adder shown in Fig.1. Boolean expression for sum and carry is given by

Sum=A xor B xor Cin eqn.1
Carry=AB+BCin+Acin ……eqn.2

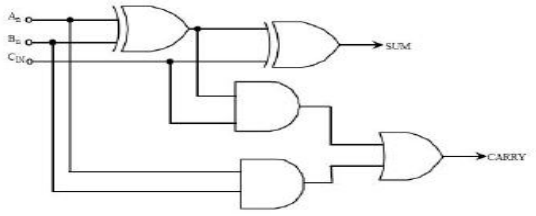

Fig. 1. Logic level diagram for full adder.

In the existing method using 14Tr full adder full swing in the sum output is achieved[1] but in carry out again there is degraded output due to 2 Tr GDI multiplexer. As carry output of full adder is also plays important role for overflow detection during arithmetic operations, 6Tr multiplexer is designed such that output should be full logic swing. Full adder using XOR is shown in Fig.2. and its simulation result using 14 Tr is shown in Fig.3. Since Full adder is a basic circuit in ALU for arithmetic operations, it is implemented with a total of 18Tr using modified GDI multiplexer. Simulated output of 18Tr full adder shown in

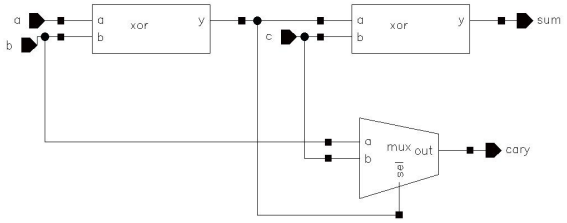

Fig. 2. XOR-MUX based full adder.

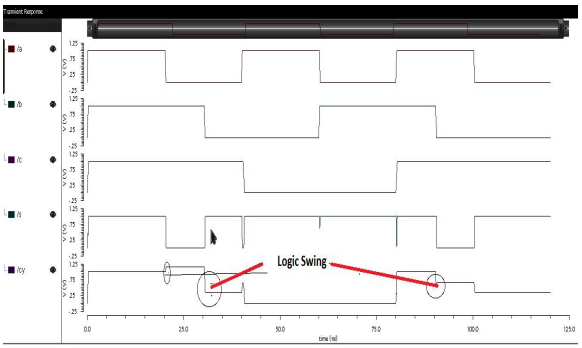

Fig. 3. Simulation of modified GDI full adder (14Tr).

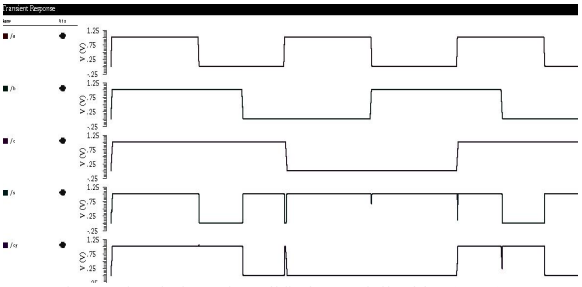

Fig. 4. Simulation of modified GDI full adder (18Tr).

The average power of this 18 Tr full adder is less compared to conventional 28 transistor CMOS and GDI full adder shown in Table I and Table 2 both 90nm and 45nm technology.

Table 1. Performance of full adder in MGDI, GDI, CMOS in 90nm technology.

90nm	CMOS [28Tr]	GDI [10Tr]	Modified GDI [18Tr]
Avg.pwr (watts)	302.0E-9	45.88E-6	396.5E-9
Delay(sec)	41.43E-12	11.36E-12	22.22E-12

3.2 Design of 4x1 Multiplexer

The proposed multiplexer is modified to obtain output with full logic swing. The 6Tr multiplexer [6] has low power and delay compared to conventional CMOS, GDI technology. Circuit level diagram of 6Tr multiplexer is shown in Fig. 5.

The proposed 4X1 multiplexer is implemented using 6Tr 2X1 multiplexer whose schematic shown in Fig. 6.

Table 2. Performance of full adder in MGDI, GDI, CMOS in 45nm technology.

45nm	CMOS [28Tr]	GDI [10Tr]	Modified GDI [18Tr]
Avg.pwr (watts)	70.23E-9	1.849E-6	49.52E-9
Delay(sec)	85.5E-12	13.22E-12	36.05E-12

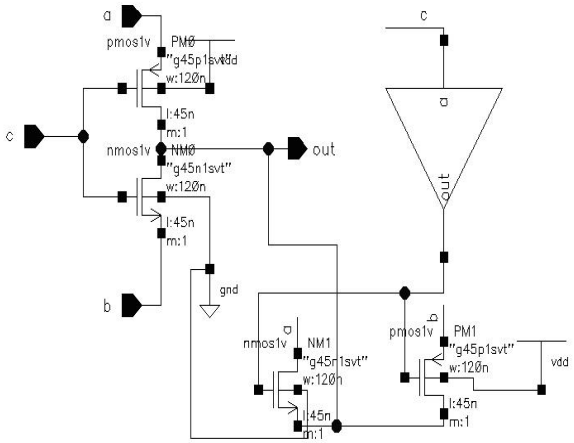

Fig. 5. Schematic view of 6 Tr 2X1 multiplexer using Modified GDI Modified GDI.

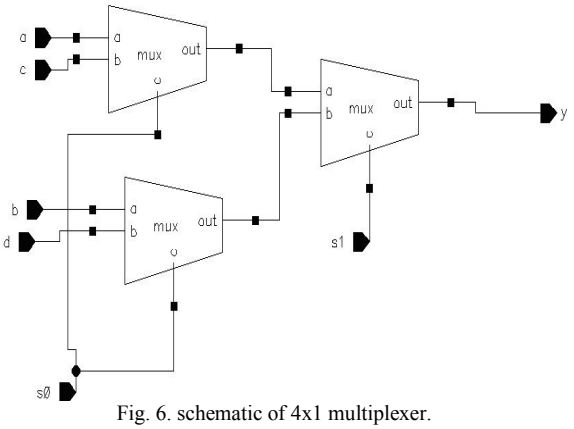

Fig. 6. schematic of 4x1 multiplexer.

3.3 Design of Shifter

Shift operations are used for serial transfer of data. They are also used in conjunction with arithmetic, logic and other data-processing operations. In a processor with many registers it is more efficient to implement the shift unit with a combinational circuit rather than sequential. A combinational circuit shifter can be constructed with multiplexers as shown in Fig.7. The 8-bit logical shifter has four data inputs, A_0 through A_3, and four data outputs Z[0] through Z[3]. There are two serial inputs, one for shift left (sl) and other for Shift Right (sr). The function table for shift operations shown in Table 3

Similarly circular shift operation is implemented. The 8-bit circular shift is shown in Fig.8.

Table 3. Function table of shift.

Select	Output							
S	Z7	Z6	Z5	Z4	Z3	Z2	Z1	Z0
Shift Left 0	A6	A5	A4	A3	A2	A1	A0	SL
Shift Right 1	SR	A7	A6	A5	A4	A3	A2	A1
Rotate Left 0	A6	A5	A4	A3	A2	A1	A0	A7
Rotate Right 1	A0	A7	A6	A5	A4	A3	A2	A1

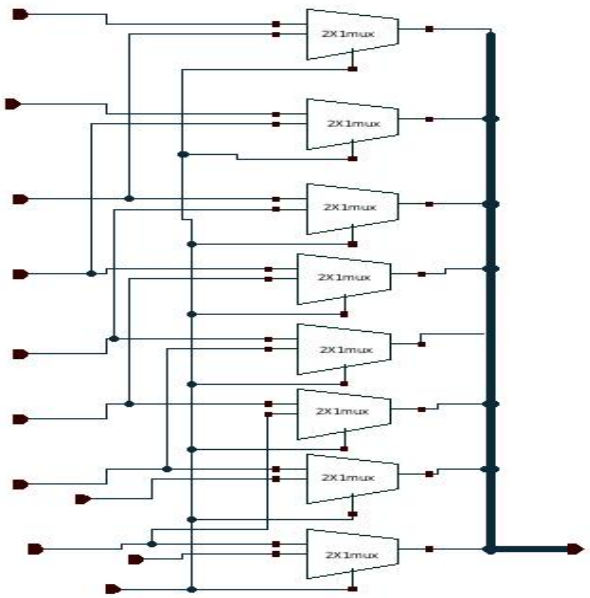

Fig. 7. 8-bit combinational circuit logical shifter.

3. 4 Design of 8-BIT Alu

The design of low power and high speed embedded systems requires that its sub components like microprocessors, microcontrollers etc. should consumes less power[5]. Arithmetic and logic unit is one of most power consuming device in processor design.

Table 4. Power and delay calculations.

Technology	GDI		MGDI	
	Avg.Pwr (watts)	Delay (sec)	Avg.Pwr (watts)	Delay (sec)
90nm	308.1E-6	137.2E-12	27.92E-6	76.17E-12
45nm	71.27E-6	161.01E-12	2.209E-6	**295**.1E-12

The existing methods used different blocks for different operations like arithmetic block, logic

block and finally outputs of each functional block given to multiplexer, which requires more area and more number of transistors, more connections, power and delay. ALU using GDI multiplexers decreases the power, area, but output is not a full logic swing and also doesn't include shift operations.

Table 5. Power w.r.t supply voltges.

Supply Voltage (V)	Power (Watts)	
	Technology	
	90 nm	45nm
0.8	11.58E-6	668.2E-9
1	12.94E-6	942.9E-9
1.2	23.92E-6	1.093E-6

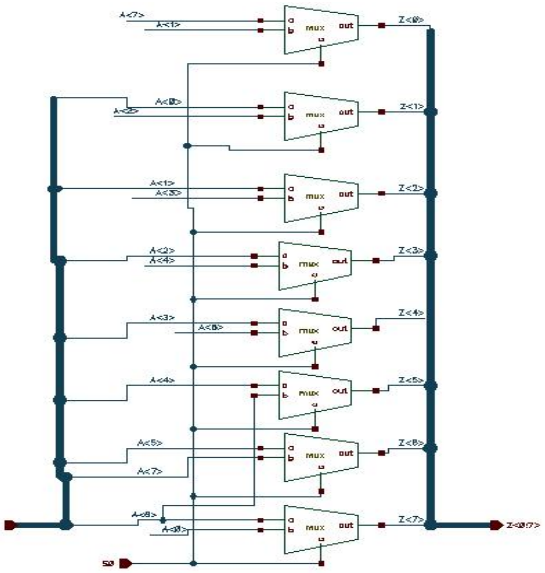

Fig. 8. 8-bit combinational circular shift.

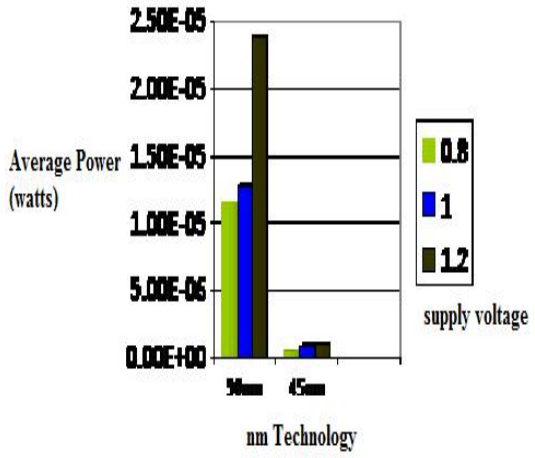

Fig. 9. Comparison of average power with various supply voltages for 90nm and 45nm technology.

Table 6. Functional table of ALU.

S3	S2	S1	S0	Cin	Output function	Operation
0	0	0	0	0	A+B	Addition
0	0	0	0	1	A+B+1	Addition with carry
0	0	0	1	0	A+B'	Substraction with borrow
0	0	0	1	1	A+B'+1	2's complement subst raction
0	0	1	0	0	A	Transfer A
0	0	1	0	1	A+1	Increment
0	0	1	1	0	A-1	Decrement
0	0	1	1	1	A	Transfer A
0	1	0	0	X	AVB	OR
0	1	0	1	X	A &B	AND
0	1	1	0	X	A'	NOT
0	1	1	1	X	A^B	XOR
1	0	0	X	X	RL	Rotate right
1	0	1	X	X	RR	Rotate left
1	1	0	X	X	SHL	shift left
1	1	1	X	X	SHR	Shift right

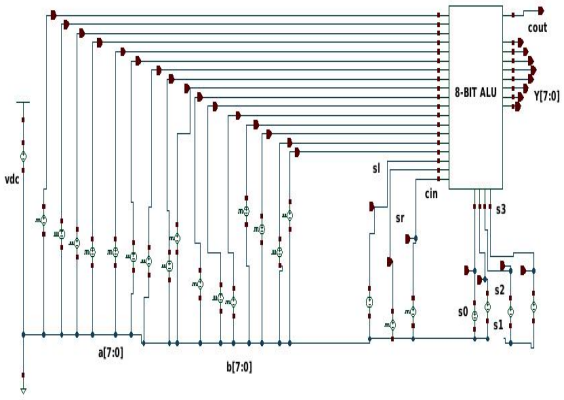

Fig. 10. Test bench schematic of 8-bit ALU.

The above said drawbacks are eliminated with the proposed technique. The proposed ALU is designed using Low power and high speed 4x1 multiplexers and Full adder using Modified GDI technique.ALU consists of four select signals S3,S2,S1,S0 and one Cin input for different arithmetic operations. Final multiplexer has S2, S3 selection lines to select four different operations of ALU [7]. Fig.13. shows schematic of 8-bit ALU.

Functional Table of ALU shown in table 6.. Compared to CMOS, GDI Modified GDI technique is low power and high speed. Simulation results are shown in Figure 10. The power calculations of GDI ALU and Modified GDI ALU in 90nm and 45nm are shown in Table 4.CMOS power and delay will be more compared to GDI and Modified GDI as number of transistors is more.

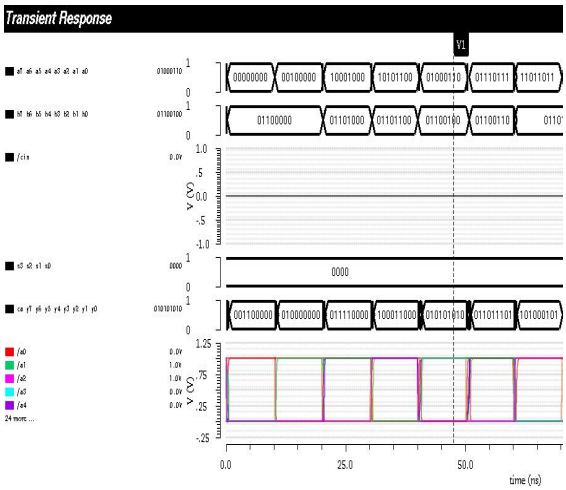

Fig. 11. Transient response of 8-Bit ALU for addition operation.

Average power dissipation with respect to 90nm and 45 nm technology for various supply voltages is shown in Table 5. The proposed ALU average power compared in 45nm and 90nm technology shown in Fig.9.from table it is observed that as supply voltage reduces power consumption also reduces i.e .voltage scaling which is one of the lower reduction techniques.

3. 5 Simulation Results

Test bench schematic of 8-bit ALU with various pulse inputs for different operations shown in Fig.10.The transient response of arithmetic, logic and shift operations shown below. The analog pulse inputs and outputs are converted into binary format using Analog to Digital conversion option in ADEL waveform window for analyzing the output.

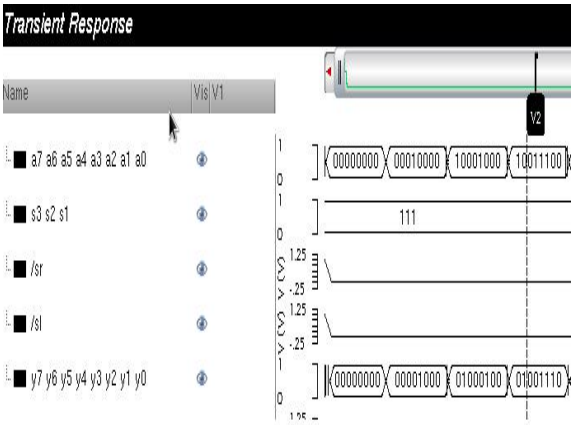

Fig. 12. Transient response of 8-bit ALU for shiftright operation

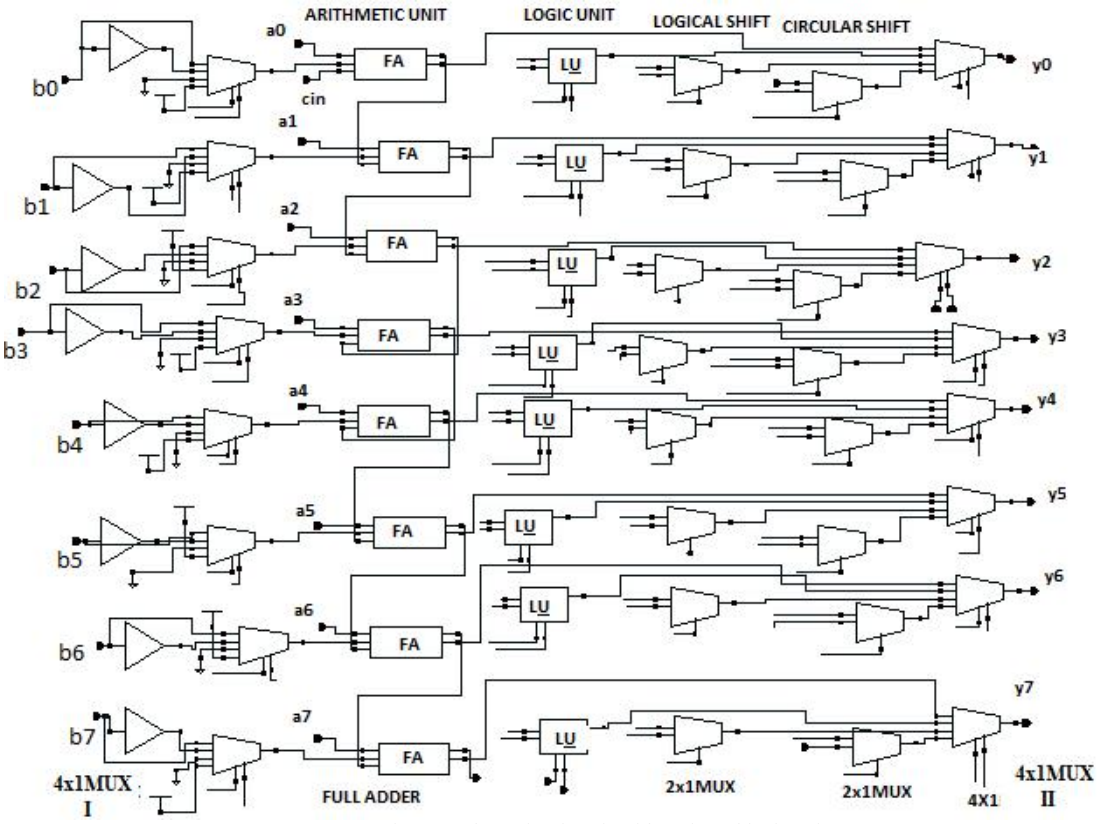

Fig. 13. Schematic of 8-Bit arithmetic and logic unit.

The 4x1 multiplexer –II [s3,s2] is used to select type of operation to be performed by ALU and 4x1 multiplexer-I [s1,s2] is used for performing seven different arithmetic Operations, cin input of full adder. Fig.11. shows transient response of addition operations with cin=0, selection input s3s2s1s0=0000 In fig.12. when selection lines of ALU [s3s3s1]=111 it performs Shift Right operation. Input data a[7:0] =00010000 then Shift Right output is y[7:0]=00001000. Similarly rotate right and XOR operation is shown in Fig.14. and Fig.15.

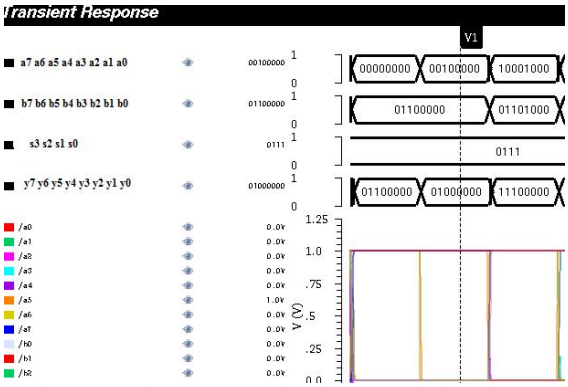

Fig. 14.Transient response of 8-Bit ALU for logic unit xor operation

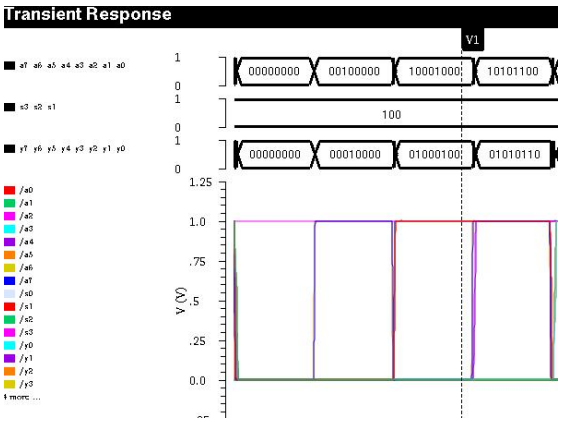

Fig. 15. Transient response of 8-bit ALU for rotate right operation

4 CONCLUSION

The high speed, low power and area optimized 8-bit ALU is designed using Modified Gate Diffusion Input Technique. Compared to CMOS technology the number of transistors was reduced. By this Power consumption, delay and area is reduced. When compared with GDI ALU, the Modified GDI ALU‘s output is full logic swing with reduced power and delay.

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