2-D Analytical Modeling of Dual-Material Double Gate Silicon-On-Nothing MOSFET

Pritha Banerjee, Aman Mahajan, Subir Kumar Sarkar

Department of Electronics &Telecommunication Engineering, Jadavpur University, Kolkata-700032, India

prithaedu7@gmail.com, amnmahajan@gmail.com, sksarkar@etce.jdvu.ac.in

Abstract: This paper presents a 2-D analytical model of Dual-Material Double Gate Silicon-On-Nothing (DMDG SON) MOSFET. In order to obtain the surface potential variation of the device, 2-D Poisson's equation with proper boundary conditions is solved. Electric field and threshold voltage are calculated for the device and the various short channel effects like DIBL, threshold voltage roll-off, hot carrier effect are examined. The close agreement between the calculated and simulated values obtained from a 2-D device simulator namely ATLAS validate the proposed model.

Keywords: Short channel effects; DIBL; threshold voltage roll-off; hot carrier effect; SOI/SON MOSFET.

1 INTRODUCTION

In the recent years there has been rigorous downscaling of MOSFETs to nanometer range to obtain faster and superior device performance [1]. But shrinking the channel length to nanometer range has made the device more exposed to Short channel effects [2]. To overcome the various Short channel effects, the conventional MOSFET structures are being continuously modified to new structures namely SOI and SON MOSFETs.Better results were obtained when Dual Gate were incorporated inthe SOI/SON structures. But the performance of DG SOI/SON MOSFETs were degraded due to HCE and Subthreshold characteristics degradation. To overcome these difficulties, multi-material gate engineering [3] has been developed where the work function of the gate material is varied and its effect on the performance of the device is studied. In this paper, using the concept of gate work function engineering coupled with SON technology, the response of the device to the various short channel effects are studied. The calculated and simulated values match well implying that the proposed model can be a promising candidate for future sub-50nm VLSI applications.

2 PROPOSED STRUCTURE AND ANALYTICAL MODELING

A schematic 2-D cross-sectional view of the proposed model namely DMDG SON MOSFET is shown in Fig.1. The work functions of the metals are ϕ_{M1} (work function of metal M1) and ϕ_{M2} (work function of metal M2). The channel length is L=L1+L2. The front oxide thickness is t_f nm, the channel thickness is t_{Si}nm and the buried air layer thickness is t_b nm.

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Considering the assumption that the channel is completely depleted under zero bias, that the impurity density and the influence of the charge carriers on the electrostatics of the channel is uniform, we have solved the 2-D Poisson's equation [4] in order to obtain the surface potential distribution of the channel.

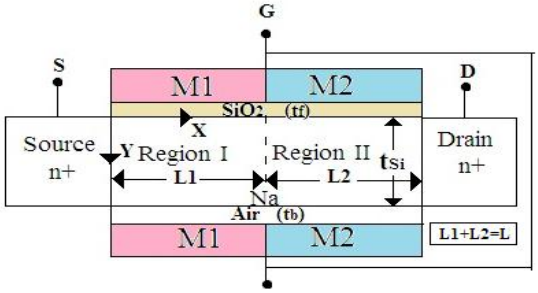

Fig.1. Schematic 2-D cross-sectional view of DMDG SON MOSFET.

$$\frac{\partial^2 \phi_1(x,y)}{\partial x^2} + \frac{\partial^2 \phi_1(x,y)}{\partial y^2} = \frac{qNa}{\varepsilon_{si}}$$

for ($0 \le x \le L1$, $0 \le y \le tsi$) (1)

$$\frac{\partial^2 \phi_2(x,y)}{\partial x^2} + \frac{\partial^2 \phi_2(x,y)}{\partial y^2} = \frac{qNa}{\varepsilon_{si}}$$

for ($L1 \le x \le L$, $0 \le y \le tsi$) (2)

where ϕ_1 (x, y) and ϕ_2 (x, y) are respectively are the potential distribution functions under M1 in region1 and M2 in region 2, Na is the uniform doping concentration in the channel, ε_{si} is the permittivity of Si and q is the electronic charge. Considering a parabolic potential approximation [5] in the channel, we can write

$$\phi_1(x,y) = \phi_{s1}(x) + C_{11(x)}y + C_{12}(x)y^2$$

(under M1)(3)

$$\phi_2(x,y) = \phi_{s2}(x) + C_{21(x)}y + C_{22}(x)y^2$$

(under M2) (4)

Here, $\phi_1(x,y)|_{y=0} = \phi_{s1}(x)$

Hence, $\phi_{s1}(x)$ is the surface potential below the front gate metal M1 at the SiO_2/Si interface in region 1 under L1 and similarly $\phi_{s2}(x)$ is the surface potential below the front gate metal M2 in region 2 under L2. In order to solve the 2-DPoisson's equation we need to consider the following boundary conditions [6] which are:

i. The tangential electric fields should be continuous at the front gate-oxide interface as well as back gate-air interface.

$$\frac{\partial \phi_1(x,y)}{\partial y} = \frac{\varepsilon_{ox}}{\varepsilon_{Si} t_f}(\phi_1(x,0) - Vgs + Vfb1)$$

(under M1) (5)

$$\frac{\partial \phi_2(x,y)}{\partial y} = \frac{\varepsilon_{ox}}{\varepsilon_{Si} t_f}(\phi_2(x,0) - Vgs + Vfb1)$$

(under M2) (6)

$$\frac{\partial \phi_1(x,y)}{\partial y} = \frac{\varepsilon_{air}}{\varepsilon_{Si} t_b}(Vgs - Vfb1 - \phi_1(x,tsi))$$

(under M1) (7)

$$\frac{\partial \phi_2(x,y)}{\partial y} = \frac{\varepsilon_{air}}{\varepsilon_{Si} t_b}(Vgs - Vfb2 - \phi_2(x,tsi))$$

(under M2) (8)

Where ε_{ax} and ε_{air} are respectively thepermittivities of SiO_2 and air, Vgs is the gate-to-source voltage, Vfb1 is the flat band voltage at the interfaces of region 1,

$$V_{fb1} = \phi_{M1} - \phi_{Si} \quad (9)$$

Vfb2 is the flat band voltage at the interfaces of region 2

$$V_{fb2} = \phi_{M2} - \phi_{Si} \quad (10)$$

where ϕ_{Si} is the work function of the uniformly doped Si channel,

$$\phi_{Si} = \chi_{Si} + Eg/2 + \phi_F \quad (11)$$

where χ_{Si} is the electron affinity of Si and Eg is the band gap of Si in eV. ϕ_F is the Fermi potential of Si,

$$\phi_F = V_t \ln\left(\frac{Na}{n_i}\right) \quad (12)$$

WhereV_t is the thermal voltage and n_i is the intrinsic carrier concentration.

ii. Potential at the source end is

$$\phi_1(0,0) = \phi_{s1}(0) = V_{bi} \quad (13)$$

V_{bi} is the built-in potential in the channel.

iii. Potential at the drain end is

$$\phi_2(L,0) = \phi_{s2}(L) = V_{bi} + Vds \quad (14)$$

Vds is the drain-to-source voltage.

iv. Potentials at the interface of the two different materials M1 and M2 is continuous.

$$\phi_1(L1,0) = \phi_2(L1,0) \quad (15)$$

$$\phi_{s1}(L1) = \phi_{s2}(L1) \quad (16)$$

Therefore, $$\frac{\partial \phi_{s1}(x)}{\partial x}\Big|_{x=L1} = \frac{\partial \phi_{s2}(x)}{\partial x}\Big|_{x=L1} \quad (17)$$

Using the boundary conditions and equation (5) in equation (3), we get,

$$C_{11}(x) = \frac{\varepsilon_{ox}}{\varepsilon_{Si} t_f}(\phi_{s1}(x) - V'gs1) \quad (18)$$

where $V'gs1$ =Vgs-Vfb1

and from equation (6) and (4) using the boundary conditions we get

$$C_{21}(x) = \frac{\varepsilon_{ox}}{\varepsilon_{Si} t_f}(\phi_{s2}(x) - V'gs2) \quad (19)$$

where $V'gs2$ =Vgs-Vfb1

Using equation (7) and (18) in equation (3) we get

$$C_{12}(x) = \frac{(1 + \frac{C_{ox}}{C_{Si}} + \frac{C_{ox}}{C_{air}})(V'gs1 - \phi_{s1}(x))}{t_{si}^{\,2}(1 + \frac{2C_{Si}}{C_{air}})} \quad (20)$$

where $C_{ox} = \varepsilon_{ox}/t_f$, $C_{Si} = \varepsilon_{Si}/t_{Si}$, $C_{air} = \varepsilon_{air}/t_b$

Using equation (8) and (19) in equation (4) we get,

$$C_{22}(x) = \frac{(1 + \frac{C_{ox}}{C_{Si}} + \frac{C_{ox}}{C_{air}})(V'gs2 - \phi_{s2}(x))}{t_{si}^{\,2}(1 + \frac{2C_{Si}}{C_{air}})} \quad (21)$$

Substituting the values of $C_{11}(x)$, $C_{12}(x)$ in equation (3) and using equation (1) and the values of $C_{21}(x)$ and $C_{22}(x)$ in equation (4) and then using equation (2) we get

$$\frac{d^2\phi_{s1}(x)}{dx^2} - \alpha\phi_{s1}(x) = \beta_1 \quad (22)$$

Where, $$\alpha = \frac{(1 + \frac{C_{ox}}{C_{Si}} + \frac{C_{ox}}{C_{air}})}{t_{si}^{\,2}(1 + \frac{2C_{Si}}{C_{air}})} \quad (22a)$$

$$\beta_1 = \frac{qNa}{\varepsilon_{si}} - \alpha V'gs1 \quad (22b)$$

$$\frac{d^2\phi_{s2}(x)}{dx^2} - \alpha\phi_{s2}(x) = \beta_2 \quad (23)$$

$$\beta_2 = \frac{qNa}{\varepsilon_{si}} - \alpha V'gs2 \quad (23a)$$

The general solution of the front surface potential function $\phi_{s1}(x)$ and $\phi_{s2}(x)$ in regions 1 and 2 can be expressed as [7]

$$\phi_{s1}(x) = Ae^{\eta x} + Be^{-\eta x} - \sigma_1 \quad (24)$$

$$\phi_{s2}(x) = Ce^{\eta(x-L1)} + De^{-\eta(x-L1)} - \sigma_2 \quad (25)$$

where $\sigma_1 = \frac{\beta_1}{\alpha}$, $\sigma_2 = \frac{\beta_2}{\alpha}$, $\eta = \sqrt{\alpha}$

The constants A,B in region 1 and C, D in region 2 can be found out using equations (13), (14), (16), (17) as,

$$A = \frac{\{(V_{bi} + Vds + \sigma_2) - (V_{bi} + \sigma_1)e^{-\eta L} + (\sigma_1 - \sigma_2)\cosh(\eta L2)\}e^{-\eta L}}{(1 - e^{-2\eta L})} \quad (26)$$

$$B = \frac{\{(V_{bi} + \sigma_1) - (V_{bi} + Vds + \sigma_2)e^{-\eta L} - (\sigma_1 - \sigma_2)\cosh(\eta L2)e^{-\eta L}\}}{(1 - e^{-2\eta L})} \quad (27)$$

$$C = Ae^{\eta L1} - \frac{(\sigma_1 - \sigma_2)}{2} \quad (28)$$

$$D = Be^{-\eta L1} - \frac{(\sigma_1 - \sigma_2)}{2} \quad (29)$$

2.1 Threshold Voltage Modeling

Threshold voltage (Vth) is that value of V_{gs} at which the surface potential minimum equals twice the Fermi potential [8]. Now the work function of M1 being greater than M2, surface potential minimum is found to occur under M1 in Region1 [as evident from the surface potential plots shown in the Section of Results and Discussions.

Now, in order to solve the position of minimum surface potential, we need to solve

$$\frac{d\phi_{s1}(x)}{dx}\Big|_{x=xo} = 0 \quad (30)$$

Now to obtain the threshold voltage we must solve

$$\phi_{s1}(xo)|_{Vgs=Vth}=2\phi_F \quad (31)$$

In this way the threshold voltage is calculated for the device.

The DIBL [8] (in mV) is given by

$$DIBL = V_{th,LIN} - V_{th,SAT} \quad (32)$$

Where $V_{th,\ LIN}$ and $V_{th,\ SAT}$ are threshold voltages in linear and saturation regions respectively.

The Electric field is calculated as

$$E = -\frac{d\phi_S(x)}{dx} \quad (33)$$

3 TYPICAL PARAMETER VALUES USED FOR DMDG SON AND DMDG SOI MOSFET

Table 1.

ϕ_{M1} (eV)	ϕ_{M2} (eV)	t_f nm	t_{Si} nm	t_b nm	N_a $\times 10^{21}$ m^{-3}	N_D $\times 10^{27}$ m^{-3}
4.8	**4.6**	**2**	**5**	**2**	**1**	**5**

ND=Source/Drain doping concentration

4 RESULTS AND DISCUSSIONS

The results obtained for the analytical model of DMDG SON MOSFET are verified using the 2-D device simulator namely ATLAS. The simulation is done considering the parameters given in Table 1.

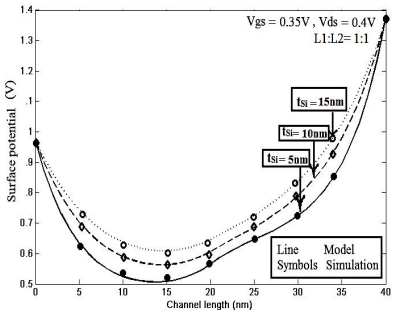

Fig. 2. Surface potential variation along the channel length for DMDG SON MOSFET for three different values of t_{Si}. The symbols in the graph represent the simulated values from SILVACO ATLAS for the proposed model considering the parameters listed in table 1.

Fig. 2 shows the variation of surface potential distribution of DMDG SON MOSET along the channel length for different values of channel thickness. It can be observed that with the decrease in the channel thickness, the step profile in the surface potential distribution of DMDG SON MOSFET becomes more pronounced which provides a better immunity of the channel towards SCE like DIBL. The step profile is a unique feature exhibited by the DMDG structures which allows the region of the channel under gate M1 to be screened from the variations of the drain voltages hence leading to a reduced DIBL effect.

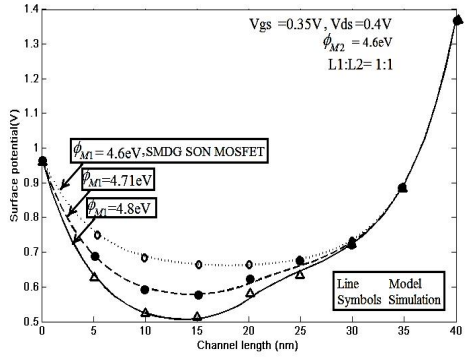

Fig. 3. Surface potential variation along the channel length for DMDG SON MOSFET for three different values of work function of M1 keeping work function of M2 fixed at 4.6eV. The symbols in the graph represent the simulated values from SILVACO ATLAS for the proposed model considering the parameters listed in table 1.

Figure 3 shows the variation of surface potential distribution along the channel length of DMDG SON MOSET for different values of work function of M1 keeping work function of M2 fixed at 4.6 eV. It can be clearly seen that the step profile in the surface potential distribution in DMDG SON MOSFET becomes more prominent , which is a desired feature to reduce DIBL, as we go on increasing work function of metal M1. This implies a better control of gate M1 over the channel. Though we can get a symmetric surface potential profile with the SMDG SON MOSFET structure (work function of M1=work function of M2, dotted curve), but the channel in that case becomes more prone to the DIBL effect because of the absence of the step profile in their surface potential distribution. The calculated and simulated values are in close agreement with each other.

Figure 4 shows the variation of electric field of DMDG SON MOSET along the channel length for different values of channel thickness. As we go on decreasing the channel thickness from 15 nm to 5 nm, the electric field gradually decreases at the

drain end which implies a reduced Hot carrier effect at the drain side. The device also exhibit a uniformity in electric field along the channel length. Hence we can state that from Figure 2 and 4, the device exhibits superior performance with smaller channel thickness.

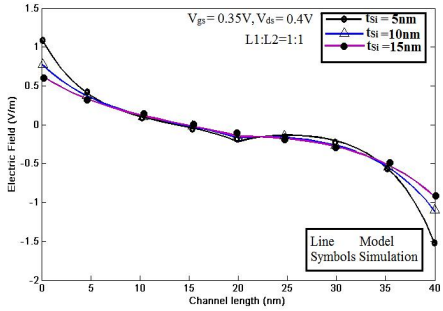

Fig. 4. Electric field variation along the channel length for DMDG SON MOSFET for three different values channel thickness. The symbols in the graph represent the simulated values from SILVACO ATLAS for the proposed model considering the parameters listed in table 1.

Figure **5** shows the variation of threshold voltage roll-off and threshold voltage of DMDG SON MOSFET with channel length. It can be observed from the figure that with the increase in L1:L2 ratio, the threshold voltage increases. This means that with the increase in the length of the gate metal with higher work function, the threshold voltage is increased and not lowered. This implies a better control of the gate M1 over the channel. Also, using different L1:L2 ratios, tuning of threshold voltage is possible. It can be also seen that the threshold voltage roll-off is minimum for the highest L1:L2 ratio among the three cases. The calculated and simulated values are very close to each other.

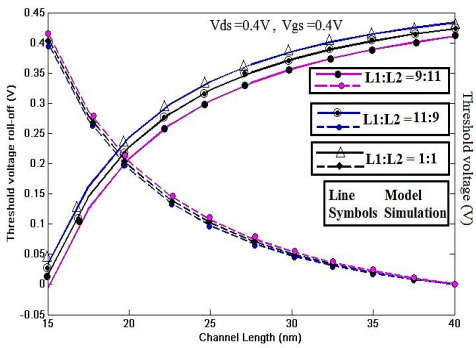

Fig. 5. Variation of threshold voltage roll-off and threshold voltage of DMDG SON MOSFET with channel length for three different ratios of L1:L2. The symbols in the graph represent the simulated values from SILVACO ATLAS for the proposed model considering the parameters listed in table 1.

Figure 6 shows the variation of DIBL with channel length for DMDG SON MOSFET. It can be observed from the that with the increase in the value of work function of the metal M1, the DIBL gradually decreases and as we move from source to drain, the DIBL value saturates to 0mV. This is because as the work function of the metal M1 is increased, the step profile in the surface potential of the device becomes more prominent hence reducing the DIBL effect in the device. It also implies a better control of the gate M1 over the channel. Figure 4 and 5 show a good agreement between the calculated and simulated values that validate our proposed model.

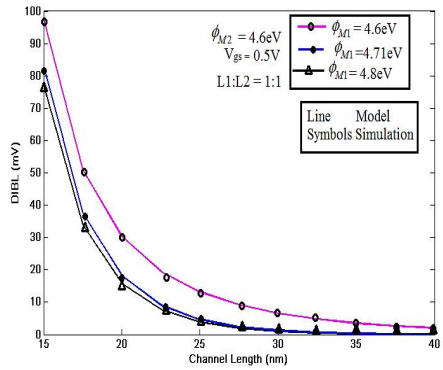

Fig. 6. DIBL variation along the channel length for DMDG SON MOSFET for three different values of work function of M1 keeping work function of M2 fixed at 4.6eV. The symbols in the graph represent the simulated values from SILVACO ATLAS for the proposed model considering the parameters listed in table 1.

5 CONCLUSION

The response of the proposed analytical model namely DMDG SON MOSFET towards the various SCEs due to channel downscaling is thoroughly studied. Its surface potential variation, threshold voltage and electric field are calculated. The unique step profile in its surface potential distribution highly contributes towards its immunity of suppressing major SCEs like DIBL, HCE, threshold voltage roll-off. The flexibility of selecting different L1: L2 ratios, work functions of the gate metals is an additional advantage that allows us to explore the different features of the proposed model. The calculated and simulated results are very close to each other hence validating our proposed model.

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