Design and Analysis of Multiplexer Based CMOS Full Adder in Conventional and Adiabatic Logic for Ultra Low Power Application in Sub-Threshold Regime

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Abstract: The growing pace and complexity of today's outlines imply a noteworthy rise in the power consumption of very-large-scale integration (VLSI) chips. We all are passionate to give the steadiness in the curve of power consumption day by day. To encounter this problem, researchers have evolved many different design approaches to minimize power. As electronic components are being blended into small, portable gadgets, the requirement increases for growing functionality, with chopped size and slighter power consumption in unit time. This suggests a requirement to stabilize ultra-low power with area-efficient design. In this paper, we explore the implementation of 1-bit full adder using 4:1 Multiplexer in sub-threshold region for ultra-low-power applications in both CMOS logic and ECRL logic. The results of the simulations show that the ECRL logics have some advantages compared to their CMOS logic counterparts of same circuit. Enhancing the execution of these circuits will guide to improvement of gross system performance.

Keywords: Full Adder; Multiplexer; Sub-Threshold; CMOS; ECRL; Ultra Low Power.

1 INTRODUCTION

The need for executing ultralow-power digital systems in large number of modern applications such as mobile systems, implanted biomedical systems and sensor network has increased the significance of designing logic circuits in sub threshold regime. These unfold applications contain low energy as the prime concern in place of interpretation, with the goal of yielding energy from the nature. Sub-threshold logic is known as effective method to gain ultralow energy per single function for low-to-medium output applications. Subthreshold operation is rising as an energy-saving method to many energy-driven applications where we are less bothered about processor speed. In sub-threshold logic, all the circuits work with a supply voltage VDD lesser than the transistor threshold voltage VT and use the leakage current as the operating current. Normal CMOS logic circuits using sub threshold transistors can naturally operate with a very less power consumption, which is literally due to the dynamic power consumption and is quadritically rely upon the source voltage as $CLfVDD^2$ (where CL is load capacitance, f is operating frequency and VDD is supply voltage).In recent times, adiabatic logic has emerged as a positive approach in strong inversion regime, to cut down dynamic power consumption importantly without offering noise immunity and driving potential. These circuits achieve ultra-low energy consumption by guiding currents across devices with less voltage differences and by slowly reusing

ISSN: 2222-7059 (print), ISSN: 2222-7067 (online), http://www.aspbs.com/aiem
DOI: 10.7508/aiem.2016.02.001

the energy conserved in their capacitive loads, mainly in low frequency regime. As the performance demands are completely lightened in many of the energy efficient sub-threshold, we feel that the adiabatic style can be used effectually in sub-threshold regime to build the circuit much more energy efficient.

On the other side, the growing pace and complexity of today's outlines imply a noteworthy rise in the power consumption of very-large-scale integration (VLSI) chips. To fulfill this challenge, researchers have unfolded many different design techniques to cut down power. Intrinsic low-power consumption of complementary metal-oxide semiconductor, or CMOS technology is one of the important features that guide to the success. This reveals that electronic design automation tools and circuit designers could sustain to concentrate on increasing circuit performance and decreasing circuit area. Another remarkable feature of CMOS technology is its great scaling properties, which has enabled a steady reduction in the feature size allowing for more and more composite systems on a single chip, which works at higher clock frequencies. In this decade, lifetime of battery is a conclusive factor for the commercial victory of the product. Another fact which became relevant at the same time was that the growing integration of more active elements contained per unit area would conduct to positively large-energy consumption of an integrated circuit. A high definite level of power is not only unwanted for economic and environmental reasons, but it also produces the problem of dissipation of heat. Appropriately to keep the device running at threshold temperature levels, huge amount of heat may require costly heat removal systems. These aspects have contributed to the hike of power as a important design parameter with performance. In fact, power consumption is considered as the boundary in the prolonged scaling of CMOS technology. To answer to this challenge, in the last decade or so, thorough research has been given into developing computer-aided design tools which address the issue of power optimization. Beginning efforts were directed to circuit and logic-level tools because at this level.

Computer-Aided-Design (CAD) tools have more developed and there is a better control on the issues. Maximizing the operating frequency, the power dissipation grows proportionally and then, minimizing the power dissipation is the main object of low power circuit design.

Our goal is to minimize the power dissipation & maximize the energy efficiency of the logic circuits. By the AC power supply the charge can be retrieved to the original power supply, which is an ease for low power circuit design. The name of the method is Adiabatic Logic. Adiabatic logic is a efficient way of minimize dynamic power dissipation. Although adiabatic circuits consume zero power theoretically, but they show nonzero power consumption for resistance in switching the transistor. But the loss of energy is very less than standard CMOS circuit. To maximize the energy effectively one computation can be introduced for reprocessing the energy which is drawn from the power supply. This adiabatic logic provides the probability of further depletion the energy dissipated in the time of switching events, and the probability of reusing some of energy taken from power supply. To fulfill this goal, the circuit diagram and the operation principles need to be modified, sometimes extremely. The amount of energy reusing executable using adiabatic techniques is also calculated by the fabrication technology, switching speed and also voltage swing. The Adiabatic Logic raises to a class of low power electronic logic circuits which brings the concept of reversible logic and also the term "Adiabatic Logic" comes from the point that the total energy or heat of the system in an adiabatic process remains constant. Similarly, for adiabatic logic circuits the energy produced in the node capacitance is recycled by the circuit in place of dissipating it, which results in notable amount of power saving as contrast to conventional logic styles.

Table 1. Truth table of full adder circuit.

A	B	C	SUM	Cr
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

In this section, behaviors of Efficient Charge Recovery Logic (ECRL) logic structure have been inspected in the sub-threshold regime for the very first time in the literature. Proposed structures are effective compared with the conventional logic circuits for very low leakage and very little amount of power dissipation. Conduction of adiabatic logic circuits has also been inspected in the sub-threshold regime for establishing ultra-low power VLSI circuits. It has been noted that the adiabatic logic circuits can work effectively in subthreshold regime also and can dissipate vey low power

compared to the CMOS logic. However the transistor count is very few in the described sub-threshold adiabatic logic (SAL) circuits, the degradation of voltage swing and fan-out can cause problems in larger system execution. However, the conduction of the Efficient Charge Recovery Logic (ECRL) has been inspected in sub-threshold regime, which contains complementary output and would be efficient in power dissipation without contributing the noise immunity and the fan out.

2 BASIC OPERATION OF FULL ADDER USING 4:1 MUX

MUX is a universal logic circuit. All logic gates and combinational circuits can be easily implemented using MUX. A 1-bit full adder using MUX can easily be implemented with the concept of function implementation table. A full adder has two outputs carry and sum. From the concept of k-map we can write sum=f(1, 2, 4, 7) and carry=f(3, 5, 6, 7). We know that Mux has 2^n input and 1 output lines where 'n' is the no. of select lines. A 4:1 MUX has 2 select lines and 4 input lines and an adder has 3 input lines. So, we use two select lines of the mux as input of the adder and we can manipulate the other input to get the output of the adder. We assume that A, B, C are the inputs of the adder. Now to implement the sum we take B and C as the select lines of the 4:1 MUX. A is connected with all the input lines of the MUX(I0, I1, I2, I3) through a NOT gate or more precisely we can say that A' is connected to all the input lines of MUX. In case of carry, B and C are used as the select lines of the MUX. I0 is connected with the GND (logic '0') and I1 is connected with VCC(logic '1'). The inverted input A relates to I1 and I2 lines. Thus, we can successfully implement a full adder using 2 4:1 mux or dual 4:1 Mux.

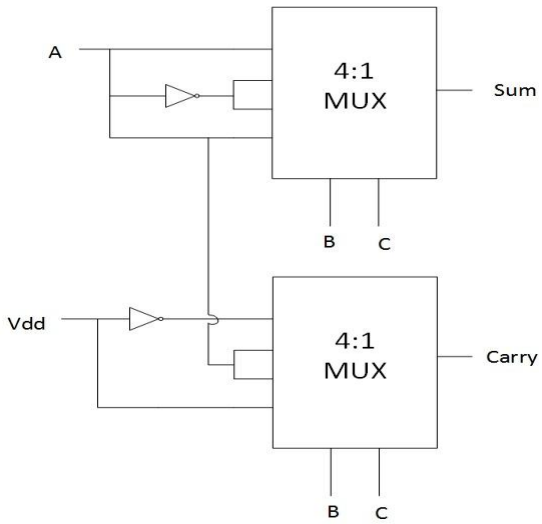

Fig. 1. Block diagram full adder using 4:1 MUX.

3 DESIGN AND IMPLEMENTATION OF 1-BIT FULL ADDER USING 4:1 MUX IN SUB THRESHOLD REGIME WITH PROPOSED STRUCTURES

The aim of this work is to provide a comprehensive study of low-power circuit and design techniques using CMOS (complementary metal-oxide-semiconductor) technology. This consists of circuit design, transistor size, number of transistors used in design, layout technique, cell topology, and circuit design for low power operation while paying particularly attention on the methodology of logic style. This paper presents, high-speed and high performance multiplexer based 1 bit adders for low-power applications such as ASIC (Application Specific Integrated Circuits), ALU (Arithmetic logic Unit). Simulations were performed by Tanner Spice for analysis of various features. The simulation results demonstrate clearly the improvement of the proposed design in terms of lower power dissipation, less propagation delay, less occupying area compared to other widely used existing adder circuits based on multiplexer.

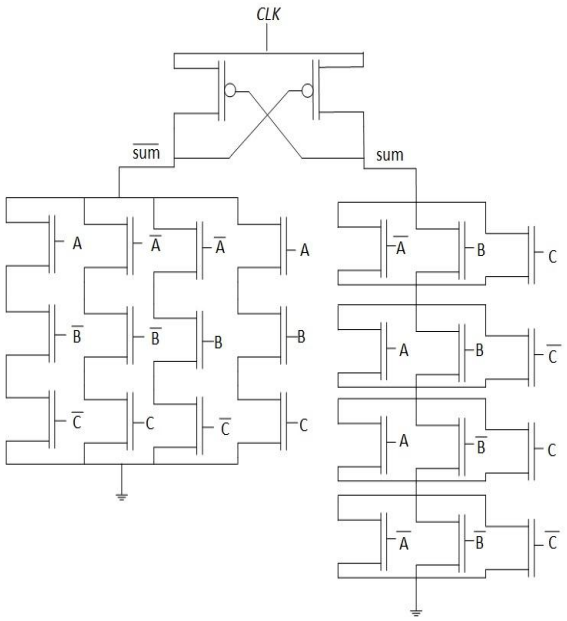

Fig. 2. Sum block of adiabatic full adder using ECRL logic.

The 1-bit full adder is one of the most critical components of a processor that determines its throughput, as it is used in the ALU, the floating-point unit, and address generation for cache or memory accesses. It is therefore inherent that full-adders have great impact on the systems that use these adders. A variety of full adders using static and dynamic logic styles have been reported in literature till now including the most well-known static complementary CMOS adders using minimum transistors. In the present work, a 1-bit full adder that utilizes a novel multiplexer-based

architecture, built upon two 4:1 identical multiplexers are used, which requires a total of 28 transistors to realize the function of a full adder. This new adder has low response time, low power utilization and reduced transition activity than previously proposed low-power adders, because it utilizes only two levels of circuit. There are three major sources of power dissipation in a digital CMOS circuit: logic transition, short-circuit current and leakage current. The following, is the low power consumption circuit adder due to reduction in short circuit current and switching activity. The short-circuit current is defined to be the direct current passing through the supply and the ground, when both the NMOS and PMOS transistors are simultaneously active, in the two-level adder, both the NMOS and PMOS transistors does not takes place simultaneously hence low transition time can be observed. All adders suffer the same short-circuit current problem as they have some internal nodes driven by signals with slow raise and/or fall times. This leads to significant (20%) short circuit power dissipation for loaded inverters. Such problem was partially solved in this design. Alongside, full adder using adiabatic ECRL is also analyzed in depth in this paper.

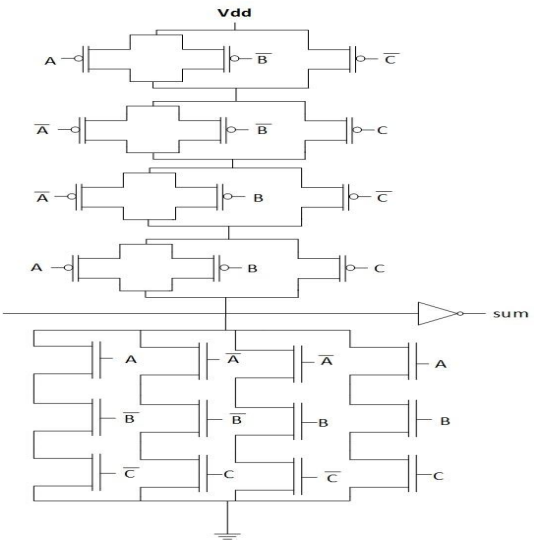

Fig. 3. Sum block of full adder using comventional CMOS logic.

Here in this paper we have tried to implement the full adder circuit using MUX and following the structures of the sum and carry blocks of the adder drawn using CMOS transistors, in ECRL logic and conventional CMOS logic. In case of ECRL logic there is an additional clock supply where we have applied a sinusoidal voltage. The proposed structures of sum and carry blocks of the conventional and adiabatic adder circuits using CMOS in sub-threshold regime using minimum number of transistors is shown here:

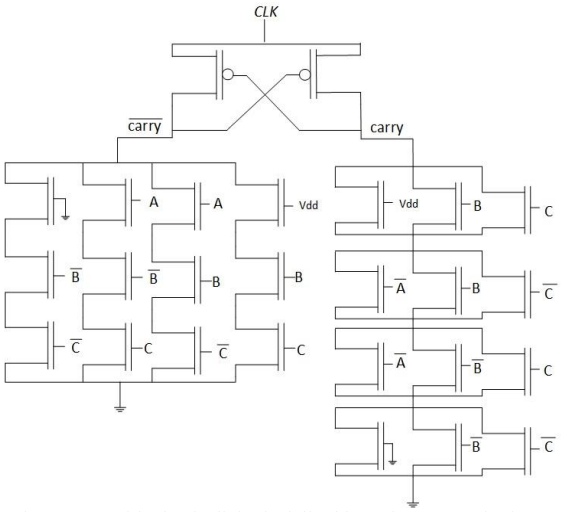

Fig. 4. Carry block of adiabatic full adder using ECRL logic.

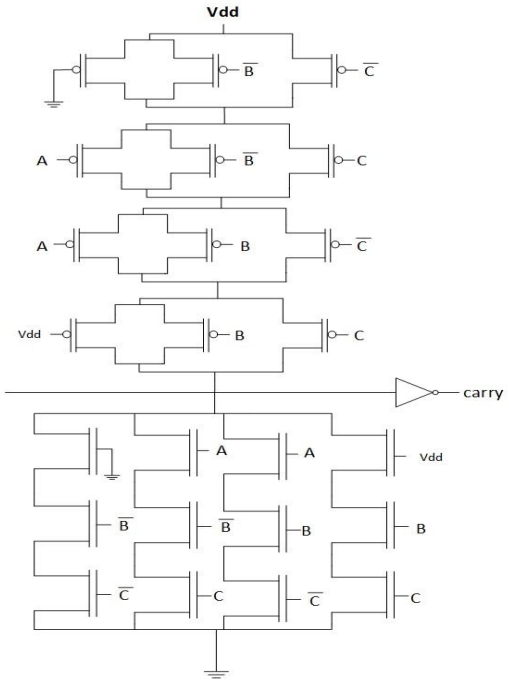

Fig. 5. Carry block of full adder using conventional CMOS logic.

4 RESULTS AND SIMULATIONS

In this paper, we have obtained the power and voltage swing characteristics of the full adder using 4:1 multiplexer by varying the supply voltage in the sub-threshold regime from 200 mV to 350 mV, by varying capacitive load from 5 fF to 50 fF and by varying temperature from -30 degree to 120 degrees. Extensive simulations have been done in this regime and we have obtained the following results and following are the plots of power and voltage swing that we have obtained by varying the above-mentioned parameters. We have simulated the code in Tanner Spice software using 22 nm technology.

In Fig. 6, we observe the variation of simulated power with change in Vdd. It is evident from the

plot that although power increases with increase in supply, the power consumed by the adiabatic full adder using ECRL logic is appreciably less than the CMOS adder. Power savings is around 89%.

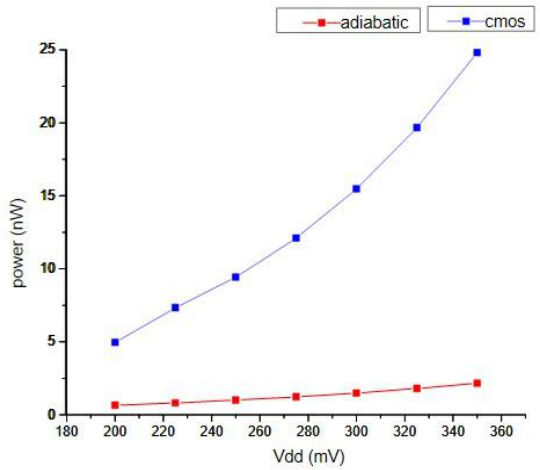

Fig. 6. Plot of Vdd (mV) versus simulated power (nW).

In Fig. 7, we have observed the change in power against change in temperature. Here also the power consumed by the adiabatic full adder is much less than the one consumed by CMOS adder and is approximately around 89.3%.

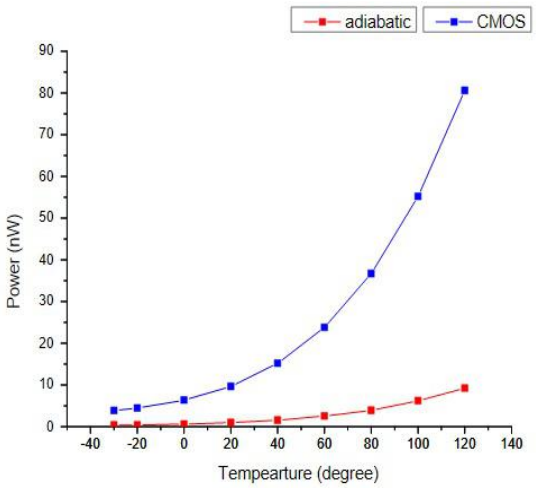

Fig. 7. Plot of temperature (deg) versus simulated power (nW).

In Fig. 8, we have observed the simulated power against variation of capacitive load (fF) is much less in case of adiabatic logic than conventional CMOS logic. Changes in both the cases in almost negligible. Savings is found to be around 56%.

In Fig. 9, we have compared the voltage swing characteristics of the CMOS and adiabatic full adder with variation in supply voltage and observed that swing with voltage variation is more with respect to adiabatic logic than CMOS logic. However, in both the cases swing increases with increase in supply. Swing is less by around 15%.

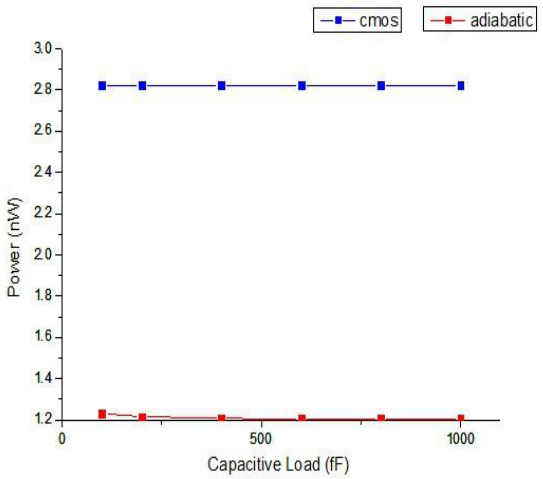

Fig. 8. Plot of capacitive load(fF) versus simulated power (nW).

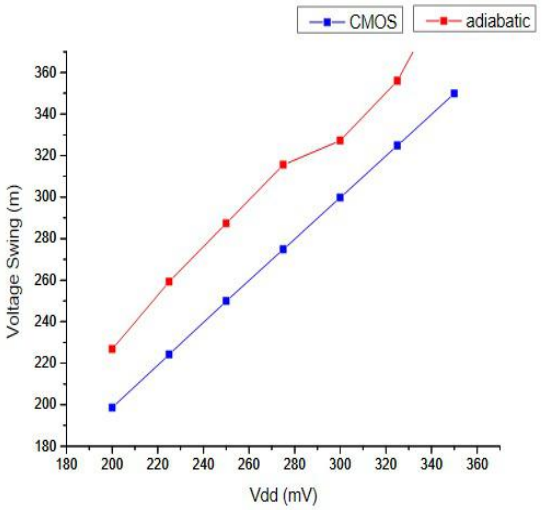

Fig. 9. Plot of Vdd (mV) versus voltage swing (m).

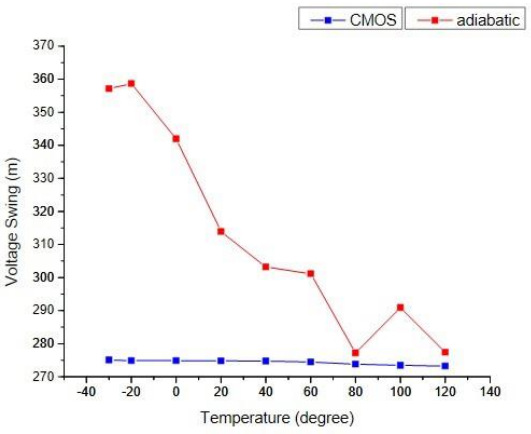

Fig. 10. Plot of temperature (degree Centigrade) versus voltage swing (m).

In Fig. 10,we tried to make a comparative study of voltage swing against temperature. In adiabatic logic, we observe that swing varies abruptly with increase in temperature whereas in CMOS logic there is very negligible variable of swing within 1mv. It is around 5.5% less than the adiabatic logic.

In Fig. 11, we tried to make a comparative study of voltage swing against capacitive load (fF). In adiabatic logic, we observe that swing varies abruptly with increase in load from 5f to 50f whereas in CMOS logic although there is an abrupt variation but is quite negligible. It is around 6% less than the adiabatic logic.

Thus, from all the simulations characteristics that we have obtained it can be inferred that for low-current driving applications sub-threshold circuits is an ideal fit in terms of power consumption. Moreover, with the application of adiabatic logic we can obtain substantial power savings in this zone compared to conventional CMOS logic. However, for appliances which can drive a large amount of current this approach may not be effective but it is promising in the other way as it has been mentioned above. Full adder using MUX has wide range of applications starting from processors manufacturing, signal processing and even in bio-medical applications.

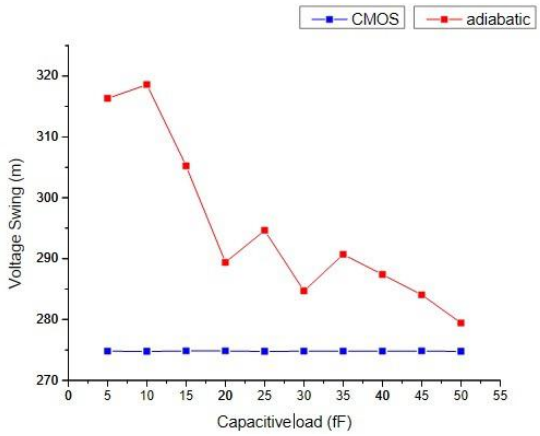

Fig. 11. Plot of capacitive load (fF) versus voltage swing (m).

5 CONCLUSION

There are some simple approaches to cut down the dynamic power such as cutting down supply voltage, minimizing physical capacitance and minimizing switching activity. These techniques are not suitable enough to encounter today's power requirement. Hence we aim on adiabatic logic, which is an efficient design for low power applications. Being known as the "energy recovery switching", adiabatic logic has made execution of transistor based logics smoother in terms of power consumption and voltage swings. Even, implementing and designing different types of logic circuits driven by this logic in Sub-threshold regime has supplied exorbitant advantages thereby minimizing the gross power consumption. Modern day scenario has observed many low power devices such as Low power microcontrollers and microprocessor such as the MSP432, Wireless Cyber peripherals, Felica-based Devices, BLE or Bluetooth Low Energy based Devices etc. Thus, as the need for low power devices tend to get importance, the concern for executing transistor-based adiabatic logic circuits has maximized. The Efficient Charge Recover Logic can be implemented in a big range of complex logic circuits which should compulsorily be driven in Sub-Threshold Regime to remarkably satisfy the necessity for low power design. This paper points to propose the new construction of adder family with two optimization goals. The first one is to access the adder in order to minimize power consumption and maximize the speed. The second one is to implement new circuit for adder to allow a production with lesser gates.

REFERENCES

[1] G. Ramana murthy, C. Senthilpari, P. Velrajkumar, and Lim tien sze, 2013. A novel design of multiplexer based full-adder cell for power and propagation delay optimizations, journal of engineering science and technology, vol. 8, no. 6, pp. 764–777.

[2] J. M. Rabaey and Pedram, M. 1995. Low power design methodologies. Kluwer Academic Publishers, Boston.

[3] M. Alito and G. Palumbo 2002. Analysis and comparison of the full adder block. IEEE Transactions on VLSI, vol. 10, no. 6, 806823.

[4] R. Shalem, E. John, and L. K. John, 1999. A novel low power energy recovery full adder cell. Proceedings of the Great Lakes Symposium on VLSI, pp. 380-383.

[5] M. Pedram and J. M. Rabaey, 2002. Power aware design methodologies. Kluwer Academic Publishers, Boston.

[6] D. Soudris, C. Piguet, and C. Goutis, 2002. Designing CMOS circuits for low power European low-power initiative for electronic system design. Kluwer Academic Publishers, Boston /Dordrecht /London.

[7] P. J. Song and G. D. Micheli, 1991. Circuit and architecture trade-offs for high speed multiplication. IEEE Journal of SolidState Circuits, vol. 26, no. 9, pp. 1119-1184.

[8] A. P. Chandrakasan and R. W. Brodersen, 1995. Low power digital CMOS design. Kluwer Academic Publishers, Norwell, MA.