



Copyright © 2016 American Scientific Publishers
All rights reserved
Printed in the United States of America

Analytical Model of Surface Potential of Double Surrounding Gate MOSFET

Abhishek Chakraborty^{a*}, Sourav Bairagya^b, Angsuman Sarkar^c

ECE Department, Kalyani Government Engineering College, Kalyani, West Bengal, India

^{a*}*chakrabortyabhishek1994@gmail.com*

^b*bairagyasourav@gmail.com*

^c*angsumansarkar@ieee.org*

Abstract: This paper presents an analytical model of surface potential of double surrounding gate MOSFET. The model has been developed using a flux-based approach. The variation of surface potentials for change in different device parameters has been provided.

Keywords: Double surrounding gate MOSFET; surface potential; analytical model; flux-based approach; short-channel effects.

1 INTRODUCTION

MOSFETs are the fundamental building blocks of modern electronic devices. In order to pack more number of MOSFETs in a single chip, we need to reduce the channel length of those MOSFETs [6]. In a conventional single Gate MOSFETs, as the scaling of the channel length reaches in the deep-submicron regime, various Short channel effects like DIBL, Hot electron effect, etc [7] becomes prominent. Again there occurs problem of trapped charge and leakage current in those devices [7]. Hence, in single Gate MOSFETs as the channel length is reduced, the MOSFET poses increasingly difficult challenges due to the deteriorating efficiency of the gate controllability to the channel [8]. Therefore, devices with multiple gate became popular in order to enhance the gate controllability. In these MOSFETs the Gate controllability is increased than single Gate MOSFETs but the device fabrication is difficult in patterning small- and high-aspect-ratio lines or pillars [1]. Again, scaling in planar bulk multigate devices is limited

upto a certain point due to the increase of parasitic effects.

To overcome these difficulties, we have proposed the model of vertical Double-Surrounding-Gate-Inner-Gate MOSFETs. These devices have reduced parasitic effects and full Gate control over the channel. So these devices can be scaled upto a large extent. Again these devices can have a very thin channel width. Henceforth, we can say that using these devices we can fabricate more number of MOSFETs on a single chip.

2 DEVICE STRUCTURE

Sl. No.	Device Parameters	Corresponding Values
1	Temperature of operation (T)	300 K
2	Intrinsic Carrier Concentration (n_i)	$1.5 \times 10^{10} \text{ cm}^{-3}$
3	Acceptor ion doping concentration (N_a)	10^{16} cm^{-3}

Continued in Next Page

Sl. No.	Device Parameters	Corresponding Values
4	Band Gap (E_g)	1.1eV
5	Permittivity of Si (ϵ_{Si})	$11.8 \times 8.854 \times 10^{-14}$
6	Permittivity of Gate Oxide (ϵ_{ox})	$3.9 \times 8.85 \times 10^{-14}$
7	Work Function of Metal Gate (W_M)	4.77
8	Work Function of Si (W_{Si})	4.68
9	Channel Length (L)	20 nm to 100 nm
10	Thickness of Inner Gate Oxide Layer (t_{OX1})	0.4 nm to 2.7 nm
11	Thickness of Outer Gate Oxide Layer (t_{OX2})	0.4 nm to 2.7 nm
12	Radius of inner Gate oxide contacts with Si (R_1)	3×10^{-9}
13	Radius of outer Gate oxide contacts with Si (R_2)	10×10^{-9}
14	A (term explained later)	0.87
15	B (term explained later)	$2.539 \times (6.5 \times 10^{-9})^{0.87}$

3 DEVICE PHYSICS AND MODELING OF DOUBLE SURROUNDING GATE (DSG) MOSFET

We have analyzed the surface potential for an n-channel undoped or lightly doped silicon ($\approx 10^{16} \text{ cm}^{-3}$) DSG MOSFET with n+ source and the highly doped ($\approx 10^{20} \text{ cm}^{-3}$) drain as shown in Fig. 1. In this case there are two surface potentials- i) Surface potential Ψ_{S1} at the inner Si-SiO₂ interface and ii) Surface potential Ψ_{S2} (at the outer Si-SiO₂ interface). The approach that is taken here to determine Ψ_{S2} (Outer Surface Potential) is to set up an elemental Gaussian volume of the silicon region in the channel with radial distance of the outer surface R_2 (outer Si-SiO₂ interface) and of the inner surface r (somewhere within the channel) and dz and $d\phi$ along axial z and angular ϕ directions, respectively as shown in Fig. 2. Here D_x denotes the electric flux density (C/m^2) with subscript x standing for the three co-ordinates r , ϕ and z , respectively. A_R , A_ϕ and A_z are surface areas (m^2) perpendicular to three directions and given by $A(R_2) = R_2 d\phi dz$, $A_r = r d\phi dz$, $A_\phi = (R_2 - R_1) dz$, and $A_z = 1/2(R_2^2 - r^2) d\phi$.

Fig. 2 also shows the incoming and outgoing flux densities along the radial r , the axial z and the angular ϕ directions, respectively. Owing to the symmetry of the structure in the angular direction, the incoming and outgoing fluxes are both the same and are equal to $D_\phi A_\phi$, resulting in zero net outward flux in the angular direction.

The outgoing flux at the outer surface of the Gaussian volume is $D_r(R_2)A_{R2}$ and the incoming flux at the inner surface is $D_r(r)A_r$. As depletion

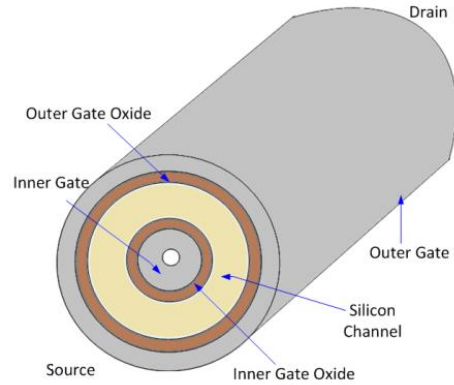


Fig. 1. Structure of a Double Surrounding Gate MOSFET.

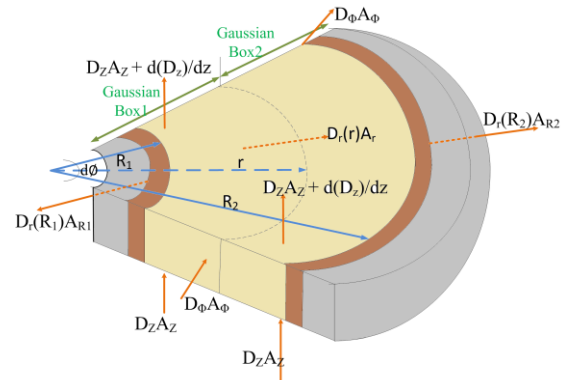


Fig. 2. Gaussian Boxes in the cross section of Double Surrounding Gate MOSFET.

charges are dominant in the sub-threshold regime, inversion charge can be neglected. Now neglecting the fringing fields at the source and the drain and applying Gauss's law to the elemental Gaussian volume in the sub-threshold regime yields the net outward flux, where dQ denotes the total depletion charge enclosed equal to the total flux lines within the elemental Gaussian volume.

$$\begin{aligned}
 F &= D_r(R_2)A_{R2} - D_r(r)A_r + \left(\frac{\partial D_z}{\partial z} dz \right) A_z \\
 &= \int_S D ds = \int_V \rho dv = dQ \\
 &= \left[\pi (R_2^2 - r^2) dz \right] \frac{d\phi}{2\pi} (-qN_a)
 \end{aligned} \quad (1)$$

As the total charge present at the outer Si-SiO₂ interface equals to the total outward flux, it is possible to write the following relation [2].

$$D_r(R_2)A_{R2} = -C_{OX2} (V'_{gs} - \Psi_{S2}) A_{R2} \quad (2)$$

where, $V'_{gs}=V_{gs}-V_{FB}$, V_{gs} is the gate-to-source voltage, and V_{FB} is the flat band voltage and is given by $V_{FB}=W_M-W_{Si}$, in which W_M and W_{Si} are work functions of polysilicon gate material and silicon channel (n-type), respectively. ϵ_{OX_2} , t_{OX_2} and ϵ_{Si} , t_{Si} are the permittivity (F/m) and thickness of the oxide and silicon, respectively, and C_{OX_2} is the oxide capacitance (per unit area), which is written as [2],

$$C_{OX_2} = \frac{\epsilon_{OX_2}}{R_2 \left(\ln \left(1 + \left(\frac{t_{OX_2}}{R_2} \right) \right) \right)} \quad (3)$$

Now, the electric field at a radial distance r in the channel is given by $E(r) = \frac{kT}{q} \left(\frac{A-2}{r} - \frac{2Ar^{A-1}}{r^A - B} \right)$. Hence, the flux entering in the Gaussian volume can be written as follows [1] :

$$D_r(r)r = \epsilon_{si}E(r)r = \frac{\epsilon_{si}kT}{q} \left(\frac{A-2}{r} - \frac{2Ar^{A-1}}{r^A - B} \right) r \quad (4)$$

In this relation A and B are two constants which are interrelated by the following equation

$$B = \frac{R_1^{1+\frac{A}{2}} + R_2^{1+\frac{A}{2}}}{R_1^{-\frac{A}{2}} + R_2^{-\frac{A}{2}}}, \text{ where } R_1 \text{ and } R_2 \text{ are the radial}$$

distance of the inner and outer Si-SiO₂ interface. Assuming the electric field is reduced to zero at the middle of the channel we get the following

$$\text{transcendental relation } \frac{2+A}{2-A} R_c^A = \frac{R_1^{1+\frac{A}{2}} + R_2^{1+\frac{A}{2}}}{R_1^{-\frac{A}{2}} + R_2^{-\frac{A}{2}}}, \text{ the}$$

solution of which gives the value of A and then using that B can be obtained. Here $R_c=(R_1+R_2)/2$. [1] We can also write

$$D_z = -\epsilon_{Si}E_z = -\epsilon_{Si} \frac{\partial \Psi_{S_2}}{\partial z} \quad (5)$$

Now using (2), (3), (4) and (5) the following relation is obtained :

$$\frac{\partial^2 \Psi_{S_2}}{\partial z^2} - \lambda_2^2 \Psi_{S_2} = \beta_2 \quad (6)$$

$$\text{where, } \beta_2 = \frac{2 \left(\frac{qN_a}{2} (R_2^2 - r^2) - C_{OX_2} V'_{gs} R_2 - D_r(r)r \right)}{\epsilon_{Si} (R_2^2 - r^2)}$$

$$\text{and } \lambda_2^2 = \frac{2C_{OX_2} R_2}{\epsilon_{Si} (R_2^2 - r^2)}.$$

The boundary potentials in the channel are:

$$\Psi_{S_2}(0)=V_{bi}, \quad \Psi_{S_2}(L)=V_{bi}+V_{ds} \quad (7)$$

where V_{bi} (Built-in-potential)= $0.56+kT/q \ln(N_a/n_i)$, $k=$ Boltzmann's Constant= 300 K. The complete solution of (6) using the conditions at (7) is given by:

$$\Psi_{S_2} = \frac{\left(V_{bi} + \frac{\beta_2}{\lambda_2^2} \right) (1 - e^{-\lambda_2 L}) + V_{ds}}{2 \sinh(\lambda_2 L)} e^{\lambda_2 z} + \frac{\left(V_{bi} + \frac{\beta_2}{\lambda_2^2} \right) (e^{\lambda_2 L} - 1) - V_{ds}}{2 \sinh(\lambda_2 L)} e^{-\lambda_2 z} - \frac{\beta_2}{\lambda_2^2} \quad (8)$$

Now, to determine the surface potential Ψ_{S_1} at the inner Si-SiO₂ interface the same approach and procedure is followed. The only change applied here is to set up an elemental Gaussian volume of the silicon region in the channel with radial distance of the outer surface r (somewhere within the channel) and of the inner surface R_1 (inner Si-SiO₂ interface), dz and $d\phi$ along axial z and angular ϕ directions, respectively as shown in Fig. 2. Considering fluxes along radial r and axial z as shown in Fig. 2. and applying Gauss's law to the elemental Gaussian volume in the sub-threshold regime yields:

$$F = D_r(R_1)A_{R_1} + D_r(r)A_r + \left(\frac{\partial D_z}{\partial z} dz \right) A_z = \int_s D ds \quad (9)$$

$$= \int_v \rho dv = \left[\pi(r^2 - R_1^2) dz \right] \frac{d\phi}{2\pi} (-qN_a)$$

where,

$$D_r(R_1)A_{R_1} = -C_{OX_1} (V'_{gs} - \Psi_{S_1}) A_{R_1} \quad (10)$$

$$D_z = -\epsilon_{Si}E_z = -\epsilon_{Si} \frac{\partial \Psi_{S_1}}{\partial z} \quad (11)$$

$$C_{OX_1} = \frac{\epsilon_{OX_1}}{R_1 \left(\ln \left(1 + \left(\frac{t_{OX_1}}{R_1} \right) \right) \right)} \quad (12)$$

$D_r(r)A_r$ can be calculated using the conditions stated in (4). Now using (4), (9), (10), (11) and (12) the following relation is obtained

$$\frac{\partial^2 \Psi_{S_1}}{\partial z^2} - \lambda_1^2 \Psi_{S_1} = \beta_1 \quad (13)$$

where,

$$\beta_1 = \frac{2 \left(\frac{qN_a}{2} (R_1^2 - r^2) + C_{OX1} V_{gs}' R_1 - D_r (r) r \right)}{\epsilon_{Si} (R_1^2 - r^2)}$$

and $\lambda_1^2 = \frac{2C_{OX1} R_1}{\epsilon_{Si} (r^2 - R_1^2)}$

The boundary condition is given by the following relations

$$\Psi_{S1}(0)=V_{bi}, \quad \Psi_{S1}(L)=V_{bi}+V_{ds} \tag{14}$$

The complete solution of (13) using the conditions at (14) is given by:

$$\Psi_{S1} = \frac{\left(V_{bi} + \frac{\beta_1}{\lambda_1^2} \right) (1 - e^{-\lambda_1 L}) + V_{ds}}{2 \sinh(\lambda_1 L)} e^{\lambda_1 z} + \frac{\left(V_{bi} + \frac{\beta_1}{\lambda_1^2} \right) (e^{\lambda_1 L} - 1) - V_{ds}}{2 \sinh(\lambda_1 L)} e^{-\lambda_1 z} - \frac{\beta_1}{\lambda_1^2} \tag{15}$$

Thus we have modeled the variation of the surface potentials Ψ_{S1} and Ψ_{S2} along the channel length.

4 RESULT AND DISCUSSION

The theoretical focus of this paper is to describe two surface potentials of the DSG MOSFET. The surface potentials of the device with the same potential applied at the two surrounding gates, are calculated and shown in the following figures for different channel lengths. Here we have used a 7nm channel width with $R_1=3$ nm, $R_2=10$ nm, $N_a=1016$ cm⁻³, $V_{ds}=1$ V, $V_{gs}=0.1$ V, $W_M=4.77$ V, $W_{Si}=4.68$ V, $t_{OX1}=t_{OX2}=2$ nm, $L=40$ nm.

Now, first the channel length is varied keeping other parameters constant and the corresponding plots are shown in Figs. 3 and 4. It is very evident that with increasing channel length the short-channel effects are becoming comparably negligible and hence the surface potential variation becomes flatter for larger values of L. In case of smaller values of L where short channel effects have their impacts the potential curve is not flat.

Now, surface potential (Ψ_{S2}) is plotted against the variation of gate-to-source potential (Fig. 5). It is evident that as V_{gs} increases, more band-bending takes places and hence surface potential also increases [7]. Here the plot is given for three different position along the channel.

Now, keeping all the parameters constant, V_{ds} is varied and the surface potentials are calculated and

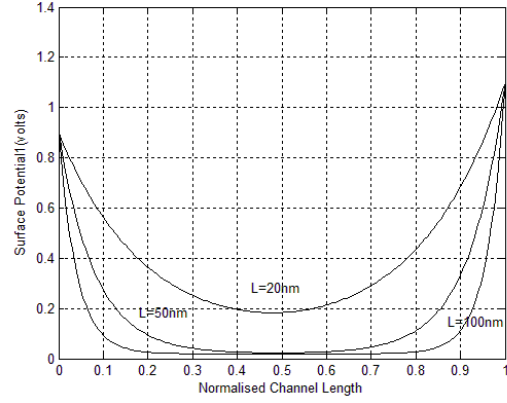


Fig. 3. Variation of Ψ_{S1} with varying channel length.

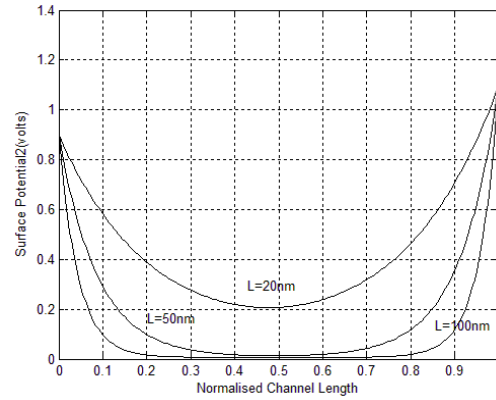


Fig. 4. Variation of Ψ_{S2} with varying channel length.

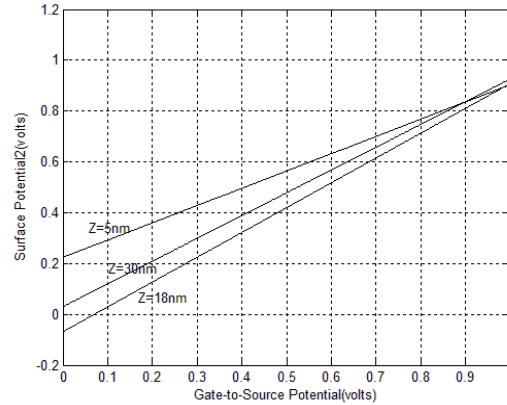


Fig. 5. Variation of Ψ_{S2} with varying gate-to-source potential.

shown (Figs. 6 and 7). As V_{ds} is increasing, the drain-induced-barrier lowering is also increasing [7]. Hence the surface potential curve is increasing much faster towards the drain end for higher values of V_{ds} .

5 CONCLUSION

In this paper we have derived a closed-form solution of surface potential for the two surfaces of the Double Surrounding Gate inner gate MOSFET. An electric flux based approach is used here to determine the two surface potentials separately. Then, various parameters like oxide thickness, drain-to-source potential, gate-to-source potential,

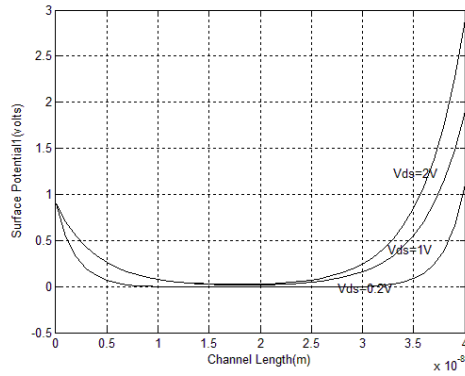


Fig. 6. Variation of Ψ_{S1} along channel length for different Drain-to-Source Voltages.

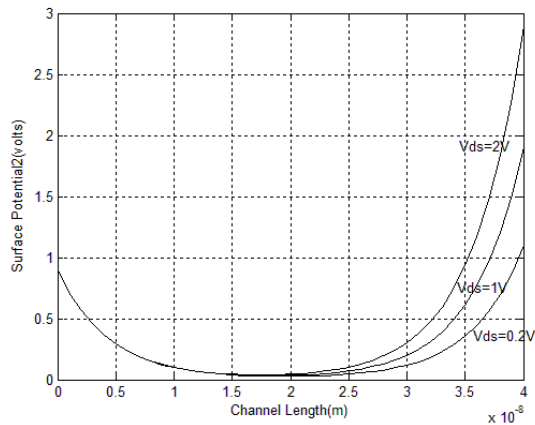


Fig. 7. Variation of Ψ_{S2} along channel length for different Drain-to-Source Voltages.

channel length are varied and the corresponding results are plotted and their explanations are given. In the derivation, one transcendental solution (4) is used. This model can be used further for surface potential based models to derive the charge and current expressions.

REFERENCES

[1] Y. Chen and W. Kang, 2012. Experimental study and modeling of double-

surrounding-gate and cylindrical silicon-on-nothing MOSFETs, *Microelectronic Engineering*, vol. 97, pp. 138-143.

[2] A. Sarkar, S. De, A. Dey, and C. K. Sarkar, 2012. 1/f noise and analogue performance study of short-channel cylindrical surrounding gate MOSFET using a new subthreshold analytical pseudo-two dimensional model, *IET Circuits Devices Syst*, vol. 6, no. 1, pp. 28-34.

[3] V.M. Srivastava, K. S. Yadav, and G. Singh, 2013. Explicit Model of Cylindrical Surrounding Double-Gate MOSFET, *WSEAS Transactions on Circuits and Systems*, vol. 12, no. 3, pp. 81-90.

[4] Y. Chen, 2007. Nanodot and nanowire transistor device modeling and fabrication process, *Jpn. J. Appl. Phys.*, vol. 46, no. 9B, pp. 6213-6217.

[5] Y. Chen and J. Luo, 2001. A comparative study of double-gate and surrounding-Gate MOSFETs in strong inversion and accumulation using an analytical model, in: *Tech. Proc. Fourth Int. Conf. on Modeling and Simulation of Microsystems*, pp. 546-549.

[6] Y. Taur and T. H. Ning, 2009. *Fundamentals of Modern VLSI Devices*, second ed., Cambridge Univ. Press, Cambridge, UK.

[7] B. G. Streetman and S. K. Banarjee, 2012. *Solid State Electronic Devices*, sixth ed., PHI, New Delhi.

[8] S. Dubey, P. K. Tiwari and S. Jit, 2010. A two-dimensional model for the potential distribution and threshold voltage of short-channel double-gate metal-oxide-semiconductor field-effect transistors with a vertical Gaussian-like doping profile, *J. App. Phys.*, vol. 108, no. 3, pp. 034518-034518-7.