Design and Average Power Consumption Analysis of 3-Stage CMOS Ring Oscillator Circuit at 32 nm Channel Length

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Abstract: This work represents the design of a 3-Stage Complementary Metal Oxide Semiconductor (CMOS) ring oscillator circuit at 32 nm channel length of MOS (metal oxide semiconductor) transistor. In order to report average power consumption across the ring oscillator circuit, power supply voltage V_{DD} has been varied keeping other parameters as fixed quantity. The value of V_{DD} is supposed to vary from 0.5 V to 1.2 V. The circuit has been simulated using Tanner SPICE (T-SPICE) tools. It is observed from the simulation results that as V_{DD} is decreasing average power consumption across the circuit also decreasing .This indicates that for low power design the value of V_{DD} needs to be reduced .The average power consumption across the CMOS ring oscillator circuit at 1 V of V_{DD} is 67.2 µW. The simulation results for average power consumption are satisfactory context to recent low power Integrated Circuit (IC) design and fabrication.

Keywords: Ring oscillator; CMOS; IC; low power; T-SPICE.

1 INTRODUCTION

The ring oscillators are closed loop device where odd numbers of identical CMOS inverters are connected [1]. The odd numbers of CMOS inverters are connected in series [2] for constructing ring oscillator. CMOS ring oscillator circuits are very popular for many digital electronics and communication applications due its easy integration. They are used as voltage-controlled oscillators (VCO's) [3-5] in many applications such as clock recovery circuits for serial data communications, disk-drive read channels, on-chip clock distribution, and integrated frequency synthesizers. It can also be used to measure the effects of voltage and temperature on a chip [6]. Ring oscillators are also used for pulse

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generator. The oscillation frequency of ring oscillator can be determined using number of inverter stage and gate delay [2]. The delay of CMOS gate can be reduced increasing V_{DD}. Therefore the frequency of oscillation of a ring oscillator can be changed varying V_{DD}. Design with low power [7, 8] is recent trends of VLSI (Very Large Scale Integration) design and fabrication .In our work power analysis of CMOS inverter has been done varying the power supply voltage V_{DD} from 0.5 V to 1.2 V at 32 nm channel length [9] of MOS transistor using T-SPICE tools.

2 DESIGN OF CMOS INVERTER

CMOS inverter is the heart of ring oscillator. The schematic diagram of CMOS inverter is shown in Fig. 1.

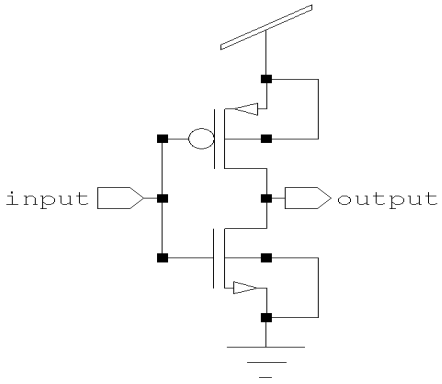

Fig. 1. Schematic diagram of CMOS inverter.

The CMOS inverter circuit has been designed and simulated at 32 nm channel of MOS transistor. The simulated voltage transfer characteristics (VTC) are shown in Fig. 2. The input and output waveforms of the inverter is shown in Fig. 3. The correctness of the functionality of CMOS inverter has been verified from the Fig. 2 to Fig. 4.

3 DESIGN OF 3-STAGE CMOS RING OSCILLATOR AT 32 nm CHANNEL LENGTH OF MOS TRANSISTOR

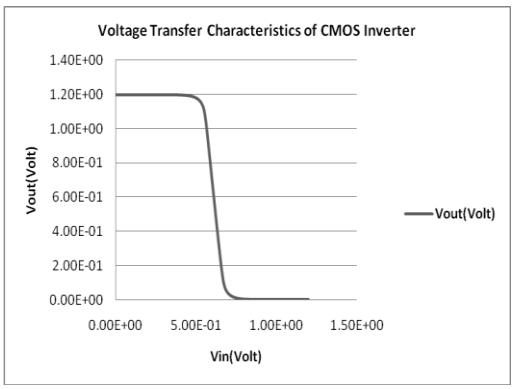

Fig. 2. Voltage transfer characteristics of CMOS inverter.

The CMOS inverter which has been designed in the previous section is used to design 3-stage CMOS ring oscillator. The Schematic diagram of the ring oscillator circuit is shown in Fig. 5. The ring oscillator circuit has been designed and simulated at 32 nm channel length of MOS transistor. The oscillating waveform from points A, B, C of Fig. 5 are shown in Fig. 6.

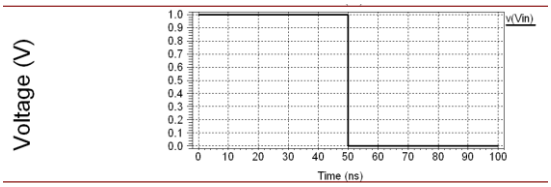

Fig. 3. Input signal to CMOS inverter.

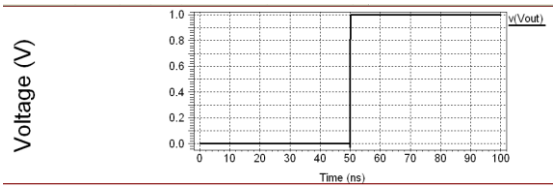

Fig. 4. Output waveform from CMOS inverter.

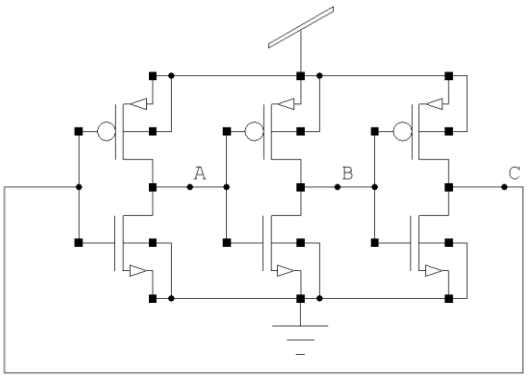

Fig. 5. Schematic diagram of 3-stage ring oscillator circuit.

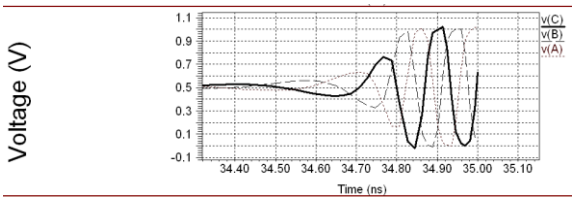

Fig. 6. Oscillating waveform at point A, B, C.

The oscillation frequency of the ring oscillator as measured from wave form is 7.69 GHz at V_{DD} of 1 V.

4 AVERAGE POWER CONSUMPTION ANALYSIS OF 3-STAGE CMOS RING OSCILLATOR AT 32 nm

Power consumption is the vital metrics for recent low power VLSI design. In our work power consumption across the 3-stage ring Oscillator circuit has been measured varying V_{DD} from 0.5 V

to 1.2 V using T-SPICE tools. Nature of Instantaneous power consumption across the ring oscillator has been presented in Fig. 7.

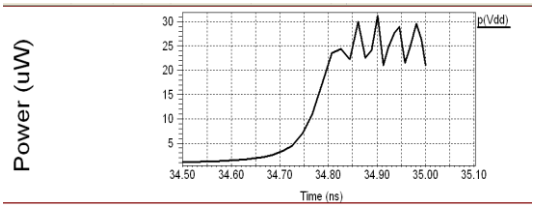

Fig. 7. Instantaneous power consumption across 3-stage ring oscillator.

The measured values of average power consumption varying V_{DD} from 0.5 V to 1.2 V are reported in Table 1. The graphical representation of the power consumption considering Table 1 is shown in Fig. 8. It has been observed that average power consumption across the circuit has been decreased due to reduction of V_{DD}. This designates that for low power design value of V_{DD} needs to be reduced .As seen from measured value average power consumption across the ring oscillator is 67.2 μW at V_{DD} of 1 V.

Table 1. Average Power Consumption across 3-Stage Ring Oscillator.

V_{DD} (Volt)	Average Power Consumption(W) Across 3-Stage Ring Oscillator
0.5	1.77E-06
0.6	6.66E-06
0.7	1.51E-05
0.8	2.76E-05
0.9	4.47E-05
1	6.72E-05
1.1	9.50E-05
1.2	1.29E-04

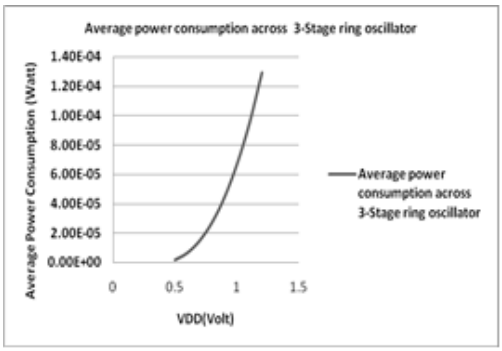

Fig. 8. Average power consumption across 3-stage ring oscillator with respect to VDD.

5 CONCLUSION

In this work 3-stage ring oscillator circuit has been designed successfully at 32 nm channel length of MOS transistor. From simulation result it is found, the oscillation frequency of the ring oscillator is 7.69 GHz at V_{DD} of 1 V. Power consumption analysis is done varying V_{DD} from 0.5 V to 1.2 V. The average power consumption across the ring oscillator circuit is 67.2 μW at V_{DD} of 1 V. The simulation results are satisfactory context to recent low power VLSI design and our design is suited for fabrication.

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