Average Power Consumption and Delay Analysis of Schmitt Trigger Circuit using Low Dimensional MOS Transistor

Surajit Bari[1a]*, Arunima Maity[1b], Debashis De[2c], Angsuman Sarkar[3d]

[1]ECE Department, Narula Institute of Technology, Agarpara, Kolkata, India

[2]Department of CSE, Maulana Abul Kalam Azad University of Technology, West Bengal,Salt Lake, BF-142, Kolkata, India

[3]ECE Department, Kalyani Government Engineering College, Kalyani, Nadia, India

[a*]*surajit9bari@yahoo.co.in*

[b]*arunima.maity27@gmail.com*

[c]*dr.debashis.de@gmail.com*

[d]*angsumansarkar@ieee.org*

Abstract: In this work the average power consumption analysis of Schmitt trigger circuit using Metal Oxide Semiconductor (MOS) transistor having channel length of 70 nm has been reported. It is found that the average power consumption is 3.3 μW at power supply voltage (V_{DD}) of 1V. The gate delay is one of the key parameter to analyze the speed of response of the Schmitt trigger circuit. In order to investigate the gate delay power supply voltage V_{DD} has been varied from 0.5 V to 1.2 V. From the simulation results it is seen that gate delay of the Schmitt trigger circuit at 1 V V_{DD} is 24 ps. The order of power consumption and gate delay for the Schmitt trigger circuit in this work is satisfactory and the values are relevant to recent low power and high speed Integrated Circuit (IC) design. It has also been observed form simulation results that as V_{DD} is decreasing power consumption across Schmitt trigger circuit decreases however gate delay increases. This indicates for low power and high speed Schmitt trigger circuit design value of V_{DD} needs to be optimized. Tanner SPICE (T-SPICE) tools have been used to design the Schmitt trigger circuit, to report its average power consumption and gate delay.
Keywords: Schmitt trigger; IC; nano; power; delay; T-SPICE.

1 INTRODUCTION

Schmitt trigger circuit is an important bi-stable device [1] used in many analog and digital electronic circuit applications [2]. Some major applications of Schmitt trigger circuit are conversion of analog signal to digital signal, reshaping of distorted square wave [3]. Conventionally Schmitt trigger circuit is configured using operational amplifier following re-generative feedback method. However in this approach the

ISSN: 2222-7059 (print), ISSN: 2222-7067 (online), http://www.aspbs.com/aiem
DOI: 10.7508/aiem.2016.01.017

major drawbacks are large area and high power requirement. In order to overcome these problem Complementary Metal Oxide Semiconductor (CMOS) Schmitt trigger has been developed. Context to present scenario of low power Very Large Scale Integrated (VLSI) circuit design [4, 5], this work represents the design of CMOS Schmitt trigger circuit at 70 nm channel length [6, 7] of MOS transistor. To report the average power consumption and gate delay across the circuit using so called low dimensional MOS transistor, power supply voltage has been varied [8, 9] from 0.5 V to 1.2 V keeping other parameters constant .

2 DESIGN OF SCHMITT TRIGGER CIRCUIT

The schematic diagram of Schmitt trigger circuit is shown in Fig. 1.

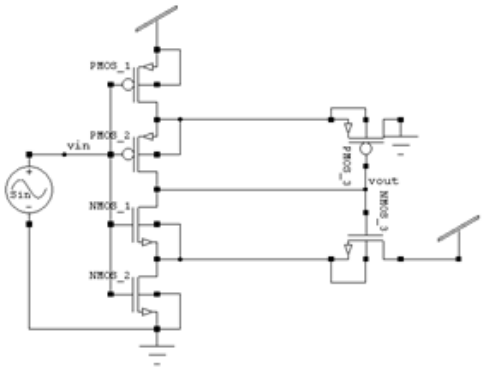

Fig. 1. Schematic diagram of CMOS schmitt trigger circuit.

The channel width (W) to channel length (L) ratio of all the PMOS in the Fig. 1 is taken as 6:1 whereas the said ratio for all the NMOS in the circuit is taken as 3:1. In order to verify the functionality, the circuit has been simulated with the help of T-SPICE tools. The input and output waveforms of Figs. 2 and 3 depicts the correctness of the design. The value of upper threshold voltage and lower threshold voltage measured from simulated waveform are 744.35 mV and 450.75 mV respectively. Therefore the hysteresis width of the Schmitt trigger is (744.35 – 450.75) mV or 294.60 mV. From Fig. 3 it is noted that during journey of positive direction when input signal crosses the value 744.35 mV, output transits from high value to low value whereas during journey of negative direction whenever input passes through the value 450.75 mV output switches from low value to high value. Fig. 3 also explains how one signal has been converted to rectangular pulse that is into digital form.

2.1 Average Power Consumption Analysis of Schmitt Trigger Circuit

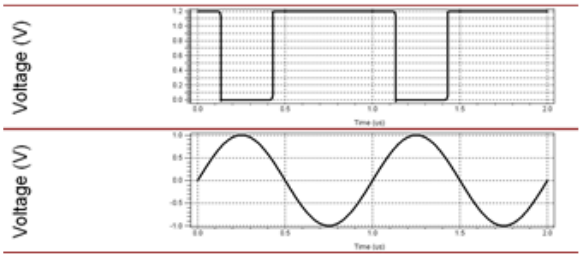

Fig. 2. Input signal –sine wave, output signal-rectangular wave.

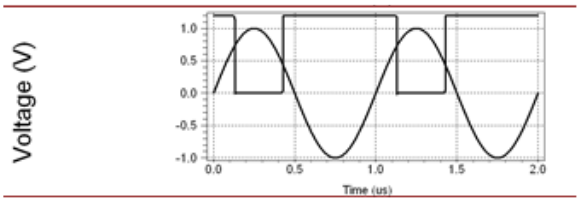

Fig. 3. Input and output wave forms. Sine wave and rectangular wave are input and output signal respectively.

Keeping other parameters constant the average power consumption across the Schmitt trigger circuit has been measured at MOS transistor channel length of 70 nm,varying V_{DD} from 0.5 V to 1.2 V. The results are reported in Table 1. The graphical representation of results from Table 1 is shown in Fig. 4.

Table 1. Average power consumption (W) across Schmitt trigger circuit at 70 nm channel length of MOS Transistor.

V_{DD}(Volt)	Average power consumption(W) across Schmitt trigger circuit at 70nm channel length of MOS Transistor
0.5	5.68E-08
0.6	1.83E-07
0.7	4.83E-07
0.8	1.05E-06
0.9	1.98E-06
1	3.31E-06
1.1	5.10E-06
1.2	7.40E-06

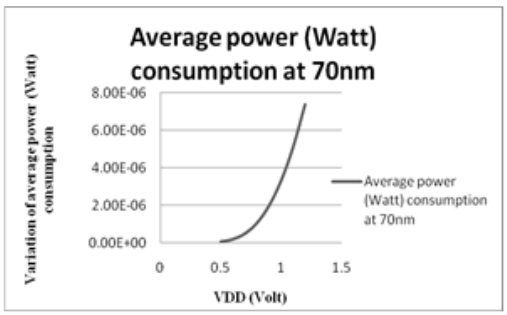

Fig. 4. The variation of average power consumption with respect to $V_{DD.}$

It is also seen from simulated waveform of Fig. 5 that the most of the power consumption occurs across the circuit during swithching event of output.

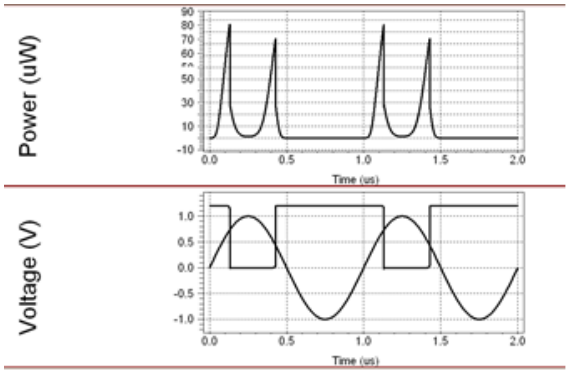

Fig. 5. Instantaneous power consumption across Schmitt Trigger circuit references to output signal (rectangular wave). Sine wave is input signal.

It is seen from Table 1 and also Fig. 4 that as V_{DD} decreasing power consumption across the circuit decreasing. Average power consumption across the circuit is 3.3 µW at V_{DD} of 1V. The results are satisfactory for low power design.

3 DELAY ANALYSIS OF SCHMITT TRIGGER CIRCUIT

To analyze the speed performance of the Schmitt trigger circuit gate delay of the circuit has been measured varying V_{DD} from 0.5 V to 1.2 V. The results are depicted in Table 2. The graphical representation of results from Table 2 has been shown in Fig. 6. It is seen from Table 2 and also Fig. 6 that as V_{DD} increasing input to output gate delay accross the circuit is decreasing. The delay across the circuit is 24 ps at V_{DD} of 1 V. The result are satisfactory for high speed design.

Table 2. Input to output gate delay at channel length of 70 nm.

V_{DD}(Volt)	Input to output gate delay (Sec)
0.5	6.62E-11
0.6	4.59E-11
0.7	3.50E-11
0.8	3.01E-11
0.9	2.74E-11
1	2.40E-11
1.1	2.19E-11
1.2	2.18E-11

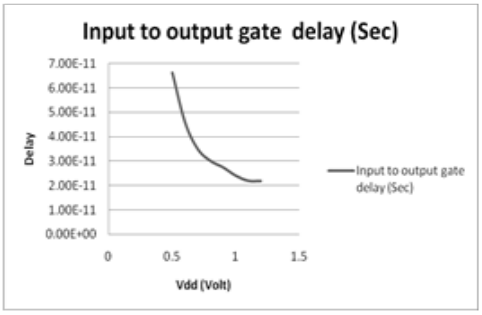

Fig. 6. The variation of input to output delay with respect to V_{DD}.

4 CONCLUSION

In this work the CMOS Schmitt trigger circuit has been designed successfully. The average power consumption and input to output gate delay has been analyzed varying V_{DD} between ranges 0.5 V to 1.2 V using T-SPICE tools. The simulated measured values correspond to average power and gate delays are satisfactory for low power and high speed VLSI design. It also noted that as power supply voltage-V_{DD} decreases average power consumption across the circuit decreases whereas gate delay of the circuit increases. Therefore for low power and high speed design the optimization of V_{DD} is necessary.

REFERENCES

[1] J. M Rabaey, A. Chandrakasan, and B.Nikolic, 2003. Digital Integrated Circuits A Design Perspective, Second Edition, India: Pearson.

[2] S. Kang and Y. Lablebici, 2003. CMOS Digital Integrated Circuits Analysis and Design, Third Edition, New Delhi, India: TMH.

[3] J. P. Uyemura, 2002. Introduction to VLSI Circuits and Systems, India: Wiley.

[4] A. Suresh, 2014. A low power Schmitt Trigger design using SBT technique in 180nm CMOS technology, International Conference on Advanced Communication Control and Computing Technologies (ICACCCT), IEEE.

[5] G. A. Raza and R. Mehra, 2015. Area and power efficient layout design of Schmitt trigger, International Conference on Computer, Communication and Control (IC4), IEEE.

[6] S.-L. Chen and M.-D. Ker, 2005. A new Schmitt trigger circuit in a 0.13-µm 1/2.5-V CMOS process to receive 3.3-V input signals, IEEE Transactions on Circuits and Systems, vol. 52, no. 7, pp. 361-365.

[7] B. Nikolic, 2008. Design in the Power Limited Scaling Regime, IEEE Transaction on Electronic Devices, vol. 55, no. 1, pp. 71-83.

[8] P. Saini and R. Mehra, 2012. A Novel Technique for Glitch and Leakage Power Reduction in CMOS VLSI Circuits, International Journal of Advanced Computer Science and Applications, vol. 3, no. 10, pp. 161-168.

[9] R. Gonzalez, B. Gordon, and M. A. Horowitz, 1997. Supply and threshold voltage scaling for low power CMOS, IEEE J. Solid-State Circuits, vol. 32, no. 8, pp. 1210-1216.