A Robust Design Optimization Technique for the Low Power CMOS VLSI

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Abstract: The paper depicts on the design optimization skills for the low power CMOS VLSI for the reliable and robust power supply entity to encourage the compactness, faster computation, power loss reductions, uncharacteristic leakages and reduction of the parasitic effects for the wider substitute of the applications. The design textures of the VLSI devices not only strengthen low power consumptions in terms of the power transfer proficiency, dynamic power, static power and the low power designing but also operate in the stable sector inside the solid integrated circuit (IC) as faster software simulation, modeling, commercial success and considerable cost effective solutions.
Keywords: CMOS VLSI; power consumption; modeling; analysis; computational speed and results.

1 INTRODUCTION

The best practicable power consumption of a particular and robust complementary metal oxide semiconductor (CMOS) become a major issue to execute productive and reliable operations. The CMOS development is widely accepted as faster and wider application for very large scale integration (VLSI) (1).

The transistor count would be twice every eighteen months as predicted by the Gordon Moore in the year of 1963. 53% compounds are annually improvement rate over 45 years. No other technology for the mankind has fully fledged so fast so long in terms of the optimal power consumption, exponential growth, faster computation, compactness, cheaper fabrication cost and cost effective solution (1)–(2).

The history (i.e. 1971) of the scaling depicts those Intel 4004 transistors are the least dimension of 10µm. The Pentium 4(i.e. 2003), transistors are with optimal size of 130 nm thus the scaling cannot carry on the perpetual activities because the transistors of the CMOS cannot be slighter than atoms of a material (3)-(4).

The chip designers seriously depend on design automation and software tools to look for fabrication gains to cope up with substantial barrier as productivity gap of the VLSI technology.

In static CMOS device, the n-MOS transistors only have to pass 0's and the p-MOS only pass 1's as the brains of positive logic so the output is always stalwartly driven and the stages of the logic are never tainted. This term is called a totally reinstated logic gate and static CMOS gates are also smarmy

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restored through commonsensical operations. Introducing the logic basics between scan cells to optimize the number of transitions are taking place inside the scan chain. The uses of the buffers of the different dimension in multi-scan routes are to be competently exasperated in a trivial and temporal swing in between the scan chains and cutback of the highest power for the scan structural design adaptation and design optimization of the low power consumption VLSI technology (5)-(6).

It is suitably entrenched on the massive multiphase troublemaker into each scan cell involving the amendment of the remarkable style of the scan cells so it is as entitled as short slip scan stalling of the VLSI architectures for trivial solutions (7)-(8).

2 LOW POWER ISSUES

2.1 Low Power Implementation of the CMOS

The safe optimal low power implementations of the CMOS highly ensure to deal with the huge repercussions and consequences inviting various practices so that it is used to assemble for the power optimization. It is continuously carried out to optimize power consumption which may minimally be engaged once in terms of the physical layout in relationship with the robust architectures of the CMOS.

2.2 Implementation Phases of the CMOS

The designer faces the substantial challenges while low power CMOS fabrications are mainly defined by the front end design. As for example, how many CMOSs or power switches are required to prevent permissible voltage drop due to problem of the synchronization and doomed crashes. The low power consumption of the CMOS implementation phases consists of the various hierarchies. These processes are also programmed through acute automatic electronic design device as mentioned below.

- Floorboards scheduling with various power areas
- Power delivery , training and steering of the CMOS
- Introduction of power gating for the low power shut off
- Position, level shifter and post isolation of the cells
- Optimization of the threshold voltage of the CMOS
- Optimization as well as multiple supply voltages
- Tree permutations and combinations of the systems
- Balancing trees of CMOS using the power optimizer
- Expert routing with shorter the route span of the process
- Power dissipation of the CMOS should be optimal in between current and voltage overlapping area during transition period and execution time
- Examination and support to be taken into consideration of the reliability and faster operation of the CMOS
- Testing should be incorporated by the power analyser
- Power consumption should be constant with evaluation
- Proper sequence and synchronization of the gate signal
- Voltage drops across the CMOS should be under control

2.3 Power & Energy Modelling of the CMOS

The CMOS device is predominantly drawn power from the peripheral power supply item through the drain voltage (V_{DD}) in accordance with pin configuration of the IC.

The instantaneous power expression in terms of the gate charges, $Q_D(t)$ and drain voltage $v_{DD}(t)$ is given as:

$$p(t) = \frac{d}{dt}\{Q_D(t)\,v(t)\} \tag{1}$$

After differentiating the Equation (1) yields as:

$$p(t) = Q_D(t)\frac{dv(t)}{dt} + v(t)\frac{dQ_D(t)}{dt} \tag{2}$$

And the drain current may be defined as the rate of flow of charge given as:

$$i_D(t) = \frac{dQ_D(t)}{dt} \tag{3}$$

Now, the combination of the Equations (1) & (3) yields as:

$$p(t) = Q_D(t)\frac{dv(t)}{dt} + v(t)\,i_D(t) \tag{4}$$

The average power over a complete cycle or time period (T) may expressed as:

$$P_a = \frac{1}{T}\int_0^T Q_D(t)\frac{dv(t)}{dt}\,dt + \frac{1}{T}\int_0^T v(t)\,i_D(t)\,dt \tag{5}$$

The Equation (5) may be simplified considering the proper limit of the integration in terms of the drain

current (I_D) and switching frequency (f_{sw}) at steady state yields as:

$$P_A = Q_D V_{DD} f_{sw} + V_{DD} I_D \quad (6)$$

The common relation between time period (T) and the switching frequency (f_{sw}) of the CMOS is written as:

$$T = 1/f_{sw} \quad (7)$$

The average energy over the complete time period (T) may be expressed using the Equation (6) at steady state yields as:

$$E_A = P_A T = Q_D V_{DD} + V_{DD} I_D T \quad (8)$$

2.4 Dynamic Power Modelling of the CMOS

The dynamic power modelling of the CMOS plays an important function to charge and discharge load capacitances (C) when the CMOS works as a static switch as shown in the Fig. 1 to predict on the faster operation.

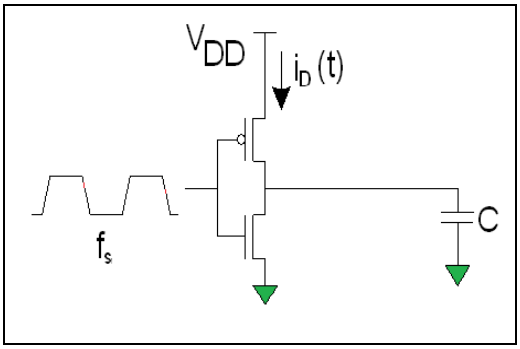

Fig. 1. Dynamic power transfer of the CMOS

Similarly, each switching cycle involves a rising and falling edge triggered of the clock pulse of the switching frequency (f_s) of the state. The capacitor (C) is charged up the supply voltage at steady state of the CMOS is given as:

$$Q_D(t) = C\, v_{DD}(t) \quad (9)$$

The charge is dumped to ground showing the green arrow in the Fig. 1. Now, arranging the Equations (5) and (9) yields as:

$$P_a = \frac{1}{T}\int_0^{V_{DD}} C\, v_{DD}(t)\, dv_{DD}(t) + \frac{1}{T}\int_0^{T} v(t)\, i_D(t)\, dt \quad (10)$$

After simplification of the Equation (10) yields as:

$$P_a = \frac{1}{2} C V_{DD}^2 f_{sw} + V_{DD} I_D \quad (11)$$

The dynamic power may be expressed with a factor as:

$$P_D = 2(P_a - V_{DD} I_D) = \beta C V_{DD}^2 f_s \quad (12)$$

When, the activation factor is considered as:

$$\beta = f_{sw}/f_s \quad (13)$$

The CMOS switch which is triggered by the clock signal is $\beta=1$ for reliable and robust operation as sizeable aspects.

The CMOS switch which is triggered by the clock signal is $\beta=0.5$, when signal CMOS turns on once per cycle over a complete time period (T) as chronological operation.

The CMOS switch turns on either "0" state or 2 times per over a complete cycle when $\beta=0.5$ is for the dynamic gates.

The CMOS switch turns on either "0" state or other states over a complete cycle when typical value of $\beta=0.1$ and it is also reliant on the prospective design for the static gates.

2.5 Short Circuit Current of the CMOS

When the CMOS transistors or switches are the combination n-MOS and p-MOS circuits may be ephemerally switched on at once. The leads to a blip of short circuit current is taken into consideration less than 10% of the dynamic power if the rising and falling edge triggered times are highly equivalent for input and output of the CMOS logics.

2.6 Example of Design Consideration I

200 M, CMOS or transistor chip and 20M logic transistors Average width: 12 unit & 180M memory of the transistors average width: 4 units, 1.2 V (DC) 100 nm process and gate capacitance, $C_g = 2f_sF$ /mm taken from the standard CMOS.

2.7 Example of Design Consideration II

Static CMOS logic gates: activation factor = 0.1
Memory arrays: activation factor = 0.05 (for many memories). Estimate dynamic power consumption per MHz when the wire capacitances affects and short-circuit current is neglected.

2.8 Example of Dynamic Consideration III

The logic capacitance of the network may be computed for using the standard data as:

$$C_L = (20\times10^6)(12\text{ unit})(0.05\mu\text{m/ unit})(2\, f_s\text{F}/\mu\text{m}) = 24\text{nF}$$

The memory capacitance may be computed as:

$$C_M = (180\times10^6)(4\text{ unit})(0.05\mu\text{m/ unit})(2\ f_s\text{F}/\mu\text{m}) = 72\text{nF}$$

Hence, the dynamic power may be expressed as:

$$P_D = [0.1C_L + 0.05C_M](1.2)^2\ f_s = 8.6\text{ mW/MHz}$$

2.9 Example of Static Power Consideration IV

The static power of the CMOS is frenzied even when chip is quiescent. Shared circuits may be burnt out by heat power in clash between turned on conditions of the CMOS. Leakage power draws during the turned off condition of the CMOS devices for the safe and secure operation.

3 RATIO PARADIGM OF THE CMOS CHIP

The CMOS chip includes a 32 word x 48 bit ROM using pseudo-n-MOS decoder and bit line pull-ups. On the average aspects, one word line and 24 bit lines are suitably taken into consideration for the robust operation in a safe zone.

The static power is smoothly drawn by the ROM as a ratio paradigm to fabricate low power CMOS for the wider faster computation and high reliability in terms of the two basic constants for the optimal design considerations, V_{DD}=1.2V.

$$\begin{bmatrix} \xi = 74.97 \quad \mu A/V^2 \\ V_\beta = 0.42\text{ V} \end{bmatrix} \tag{14}$$

The pull up current is contributed to the CMOS to compute the pull up power as per following equation as:

$$P_P = V_{DD}\left(V_{DD} - V_\beta\right)^2 \xi/2 \tag{15}$$

The expression of the pull up current is given as:

$$I_P = \left(V_{DD} - V_\beta\right)^2 \xi/2 = 22.80\ \mu\text{A} \tag{16}$$

Hence, the pull up power may be computed using the Equation (15) given as:

$$P_P = V_{DD}\left(V_{DD} - V_\beta\right)^2 \xi/2 = 27.37\ \mu\text{W} \tag{17}$$

The value of the static power for the specified ROM mentioned above given as:

$$P_s = (31+24)\ 27.07\ \mu\text{W} = 1.5\ \text{mW} \tag{18}$$

3.1 Example of Leakage Power Consideration I

The process has two threshold voltages and two oxide thicknesses.

Sub- threshold leakage effects: 20 nA/mm for low voltage, 0.23 and 0.02 nA/mm for high voltage 0.54V. Gate leakage effects: 3 nA/mm for thin oxide and 0.002 nA/mm are used for the quite thick oxide coating. The chip memories use low-leakage transistors everywhere and the logic uses low-leakage transistors on 80% of logic operation.

If the CMOS is worked out by faster computing cycle, the growth of the CMOS will be unsaturated for the applications.

3.2 Estimation of the Leakage Power

The estimation of the leakage power of the CMOS chip may be computed in terms of the leakage effects. For the high leakage effects as computed:

$$(20\times10^6)(0.2)(12\text{ unit})(0.05\mu\text{m/ unit}) = 2.4\times10^6\mu\text{m}$$

For the low leakage effects as computed,

$$(20\times10^6)(0.8)(12\text{ unit})(0.05\mu\text{m/ unit}) + (180\times10^6)(4\text{ unit})(0.05\mu\text{m/ unit}) = 45.6\times10^6\mu\text{m}$$

The static current of the CMOS may be commutated using empirical formulae using the section (V) as:

$$I_s = (2.4\times10^6\mu\text{m})[(20\text{nA}/\mu\text{m})/2 + (3\text{nA}/\mu\text{m})] + (45.6\times10^6\mu\text{m})[(0.02\text{nA}/\mu\text{m})/2 + (0.002\text{nA}/\mu\text{m})] = 32\text{mA}$$

The static power may be commutated using the following common equation:

$$P_s = I_s V_{DD} = 32\text{ mA}\ (1.2\text{ V}) = 38.4\text{ mW}$$

The heat power is generated during the execution and the wider performance parameter of a CMOS circuit is directly proportional to the dissipated power and it is highly is answerable for the die temperature increase. Too excessive temperature increase may be aggravated irrevocable structural huge degradations of the CMOS.

Too excessive high temperature may affect circuit performance or may have an impact on the ICs reliability, impingement and joule effects. The hot carrier related induced imperfections and dielectric breakdown may be incorporated for best possible power loss and low power consumption.

3.3 Low Power Data Compression

Big data and dimension highly leads to a quite power requirement for the signal processing and it may go beyond the limitation of the memory depth of the CMOS architectures. The data storage compression involves encoding a set so as to decrease its dimension. The CMOS is unlimited to storage memory and bandwidth gap between the faster computation and the memory architectures may therefore be overcome using compressed data transfer brings about to have CMOS decoder which decompresses the data as low power data density techniques. These are additional fundamental to simultaneously decrease quite the scan power loss and data volume during execution and connoisseur aspects.

The CMOS basic logic intelligence is fed into the scan sequence totally held constant. It also reduces a number of the transition states in the scan chain for the programmable elucidation to trade-off between big data compression and the execution power reduction.

Based on the huge fundamental resources of the communication, the same values to the multiple scan segments improve the robust scan structural design by keeping away from the constraint of having to have the whole segments compatible to advantage from the segmentation. The data processing power is reduced as segment wise which are incompatible during the execution to upload a given directives are not needed for the operation of the CMOS. Tradeoffs for power minimally add another axis for the design gaps. While conventional process is a trade offs between frequency and its area. Challenges of power supply is an another restriction in designing the layout is going forward

3.4 Switching Power Loss of the CMOS

The switching power loss of the CMOS comes into play to drag the temperature so it should be managed by the heat sink to restrict the temperature rise of the CMOS architecture. The switching power takes place due to overlapping condition of the current and voltage stress during turned on and turned off of the static CMOS switch respectively.
The switching power loss may be expressed in terms of the rise time (t_r) and fall time (t_f) of the peak voltage and current of the main CMOS as switching waveforms as shown in the Figs. 2 and 3 at steady state given as:

$$P_{ss} = \left[(V_{DD} I_D)/6 \right] (t_r + t_f) f_s \qquad (19)$$

If the summation of the rise time and fall time of the clock pulse tends to zero, the switching power will also tend to zero for faster operation and no data transmission loss as:

$$P_{ss} = \underset{(t_r + t_f) \to 0}{\text{Lim}} \left[\frac{V_{DD} I_D}{6} (t_r + t_f) f_s \right] = 0 \qquad (20)$$

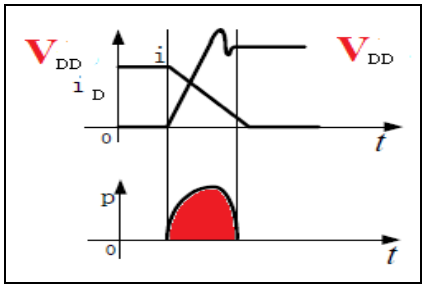

Fig. 2. Switching characteristics of the CMOS.

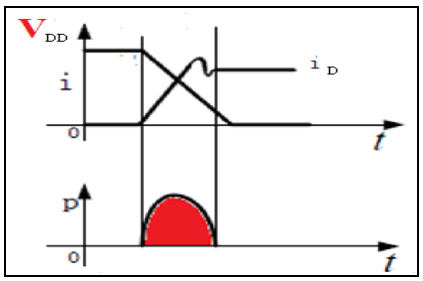

Fig. 3. Switching characteristics of the CMOS.

3.5 Conduction Power Loss of the CMOS

The conduction power loss (P_c) of the power CMOS comes into play due to rms current of the source, $I_{D\ (rms)}$ and on time resistance (R_{ds}) and during on time (t_{on}) of the CMOS over complete cycle (T) is given as:

$$P_C = \frac{1}{T} \int_0^{t_{on}} I^2_{D(rms)} R_{ds} dt = I^2_{s(rms)} R_{ds} \frac{t_{on}}{T} = I^2_{D(rms)} R_{ds} D \qquad (21)$$

When the duty cycle of the gate pulse may be defined for the faster CMOS operation given as:

$$D = t_{on}/T = t_{on} f_s \qquad (22)$$

3.6 Results

The supply voltage of the CMOS is abridged in the recent processes for saving power and for the faster computation and wider range of applications. The high supply voltage damages newest tiny transistors or the CMOSs.

The supply voltage versus power consumption curves or graphs are for the three set of frequency (1.1 GHz, 2.2 GHz & 3.3 GHz) as shown red, blue and yellow colour in the Fig. 4 respectively which predicts the voltage ranges between 1.1 to 1.2 V operating under the linear and capable zone,

distortion less, noise free, negligible effects of the parasitic components, high speed of operations and constant power consumption of the CMOS so it may be treated as optimization supply voltages for the different clock frequencies. It is also verified by the Matlab simulation result.

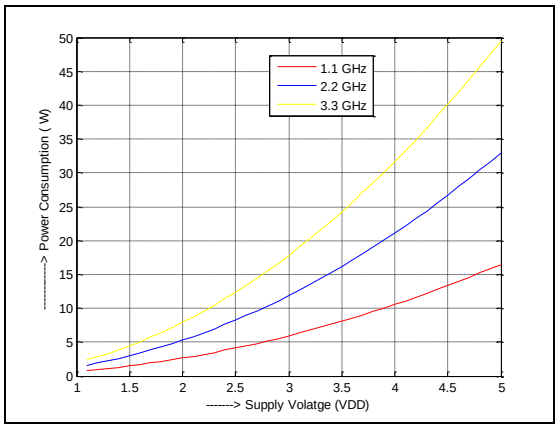

Fig. 4. Supply voltage vs. power consumption graphs for the different frequency of the CMOS.

3.7 Conclusions

The supply voltages of the CMOS circuit should be chosen 1.1 to 1.2 V (DC) for optimal power consumptions, efficient ranges, linear sector, less power loss, robust and consistent operation and faster computational speed. These predictions are best suited for the wider range of the practical applications as an improved performance of the low power CMOS VLSI.

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