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An Investigation of Performance Analysis of a Nanoscale Ge Source MoS2 Channel Tunnel FET

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Abstract: An attempt is made to analyze theoretically a Tunnel FET with Ge as the source material and atomically thin MoS_2 as channel material. The transition metal dichalcogenides (TMDs) have attracted considerable interest for using as channel material for FETs, specifically for mitigating the degradation of device electrostatics. This is due to their ultra-thin planer two-dimensional structure which is also easy to fabricate compared to one-dimensional structures (such as nanowires and nanotubes). In this work the Ge is chosen as the three-dimensional source materials for its low band gap as needed for high band to-band tunneling (BTBT) while high band gap two dimensional bilayer molybdenum disulfide (MoS_2) to achieve low OFF-sate current. The Performance of the device is investigated theoretically developing a model for the I-V characteristic. Several performance improvements is envisaged relative to conventional III-V and Si based TFET in terms of current ON-OFF ratio, subthresold swing and gate capacitance .

Keywords: MoS2; Tunnel FET; VLSI; device technology.

1 INTRODUCTION

The two-dimensional (2D) semiconducting materials like molybdenum disulphide (MoS_2) and tungsten diselenide (WSe_2), commonly called transition metal dichalcogenides (TMDs), have gained considerable attentions for use as a future channel material in tunneling FET because of their ultra thin structure and tunable band gap and ease of fabrication[1-3]. They are increasingly used for display electronics [4] and FET-based bio/gas sensors [5], because of their non zero band gap, flexibility and dangling-bond-free interfaces. Many experimental efforts are made so far to demonstrate the superior and improved TFET performance [6, 7] and to eradicate the critical practical issues [8]. In this work a compact physics based theoretical model is developed for a tunnel FET with Ge as source material and bilayer MoS_2 as channel material suitable for circuit exploration and wide-scale applicability of these two dimensional field effect transistors.

2 DEVICE STRUCTURE AND MODEL

The device structure considered here is a single gated p-type FET with 3-D n^+ -Ge as source material while ultra thin bilayer (1.3 nm) MoS_2 is used as the channel and drain material. Germanium (Ge) is chosen as source 3D material because it has a relatively low electron affinity (EA =4 eV) and bandgap $E_{g,Ge}$ (=0.66 eV) and hence provides the

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increased BTBT probability and the use of a 2D MoS_2 (EA=4.25 eV and $E_{g,TMD}$=1.6 eV) is used as the channel which produces not only excellent electrostatics but also a small tunnelling barrier width or tunnelling distance (evaluated from the thickness of the channel), as required to increase the BTBT current.

The energy band profile along the MoS_2 channel (assumed in the *y*-direction) for a BTBT (band-to-band-tunneling) p-FET is shown in Fig. 1. In Fig. 1 the E_{FD} and the E_{FS} are the drain and source electrochemical potentials, respectively, with $E_{FD} > E_{FS}$ (applied voltage is negative at the gate) .Without negative gate bias the carrier flow is prevented due to the energy barrier created by the bandgap $E_{g,TMD}$ of the MoS_2 channel. When appropriate negative gate bias is applied, the top of the valence band inside the channel ($E_{V,\mathrm{channel}}$) goes above the bottom of the conduction band within n+Ge source region ($E_{C,\mathrm{source}}$), an energy pass window is created. Significant amount of tunneling current can flow across the reverse biased source junction if sufficient longitudinal electric field is provided by the applied bias. The bottom of the conduction band on the n^+ Ge region ($E_{C,\mathrm{source}}$) is aligned below E_{FS} by an energy offset of E_d (= $E_{FS} - E_{C,\mathrm{source}}$). With negative gate bias, the created energy pass band between the top of the intrinsic valence band ($E_{V,\mathrm{channel}}$) and $E_{C,\mathrm{source}}$ is defined as $\Delta\Phi(= E_{V,\mathrm{channel}} - E_{C,\mathrm{source}})$ and as is shown in Fig. 1. The $\Delta\Phi$ increases only with the applied negative gate voltage when the device is operating in superthreshold, and $\Delta\Phi$ does not get modulated enough by the drain potential due to negligible drain-induced barrier lowering. In our case, the threshold voltage (V_th) is defined as that particular gate-to-source potential (V_{GS}) when $E_{V,\mathrm{channel}}$ gets perfectly aligned with the $E_{C,\mathrm{source}}$ (or in otherwords $\Delta\ \Phi = 0$ eV). For a negative $\Delta\Phi$, the device is said to operate in subthresold. The threshold voltage (V_th) then can be defined as

$$V_{th} = V_{ox} + \frac{E_{g,TMD}}{2q} - \frac{E_d}{q} \qquad (1)$$

where $E_{g,TMD}$ is the band gap of the MoS_2 and V_{ox} is the voltage drop across the oxide layer under the gate. Assuming ballistic transport the BTBT current in the ON state can be calculated using the Landauer's formula as

$$I_{on} = q \int_{E_{C,\mathrm{source}}}^{E_{V,\mathrm{channel}}} T_{BTBT}(E) D_{2,TMD}(E)[f_S(E) - f_D(E)] v_y(E) dE \qquad (2)$$

where $T_{BTBT}(E)$ is the BTBT transmission probability at the source, $D_{2,TMD}(E)$ is the quantum well dimentional (2-D) density of states (DOS) of the bilayer MoS_2, $v_y(E)$ is the carrier velocity resolved in the y-direction, and q and h are, respectively, the electronic charge, and Planck's constant and $f_S(E)$ and $f_D(E)$ are, respectively, the source–drain Fermi distribution functions expressed as [9]

$$f_{S/D}(E) = \frac{1}{1 + \exp\left(\dfrac{E - E_{FS/FD}}{kT}\right)} \qquad (3)$$

k being the Boltzmann constant. Now, $D_{2,TMD}(E)$ and $v_y(E)$ may be written as

$$D_{2,TMD}(E) = \frac{m^*{}_{TMD}}{2\pi \mathrm{h}} \qquad (4)$$

$$v_y(E) = \frac{1}{\mathrm{h}} \frac{\partial E}{\partial k_y} = \frac{\mathrm{h}^2}{m^*{}_{TMD}} \left(\frac{2m^*{}_{TMD}}{\mathrm{h}^2} \right)^{1/2} E^{1/2} \qquad (5)$$

Inserting these values of eq. (4) and (5) into eq. (2) and noting that $T_{BTBT}(E)$ is constant at a particular gate and source bias, and can be taken out of the integral. Performing the integration over the energy pass window the BTBT ON current expression gets simplified as

$$\begin{aligned} I_{on} &= \frac{q(2m^*{}_{TMD})^{1/2}}{2\pi} T_{BTBT}(E) \\ &\left\{ \left[F_{1/2}\left(\frac{E_{C,\mathrm{source}} - E_{FS} + \Delta\Phi}{kT} \right) - F_{1/2}\left(\frac{E_{C,\mathrm{source}} - E_{FD} + \Delta\Phi}{kT} \right) \right] \right. \\ &\left. - \left[F_{1/2}\left(\frac{E_{C,\mathrm{source}} - E_{FS}}{kT} \right) - F_{1/2}\left(\frac{E_{C,\mathrm{source}} - E_{FD}}{kT} \right) \right] \right\} \end{aligned} \qquad (6)$$

where $F_{1/2}(\cdot)$ is the Fermi-Dirac integral function. With the objective to express the I_{on} in terms of the intrinsic parameters of the TFET and the applied bias, the transmission probability of triangular potential barrier for the atomically thin planer channel, using the WKB approximation, can be written in the following form

$$T_{BTBT}(E) \cong \exp(-\alpha \frac{\lambda_s}{E_{g,Ge} + \Delta\Phi}) \qquad (7)$$

where $\alpha = 4\left(E_{g,Ge}\right)^{3/2} \sqrt{2m^*{}_{Ge}} / 3q\mathrm{h}$ and the tunneling barrier width or average tunneling thickness

λ_s is given by

$$\lambda_s = \sqrt{\frac{2\Phi_S}{qN_s}\left((\Phi_{bi} - \Delta\Phi\right) - \frac{2kT}{q}} \qquad (8)$$

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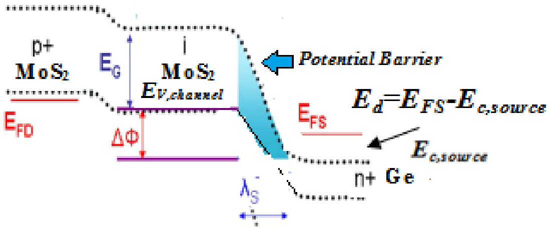

Fig. 1. Energy band profile of a Ge/MoS$_2$ tunnel-fet.

2.1 OFF State Current Model

In the OFF state, electrons from the conduction band of Ge cannot transport to MoS$_2$ because there is no DOS available in MoS2 valence band. At lower energies, in the forbidden gap of Ge no DOS is available in Ge, though empty DOS is available in MoS2, thus forbidding the flow of current in such case. With a further decrease in energy reaching below the valence band of Ge, DOS is available in both Ge and MoS$_2$. However, the number of holes available in the valence band of the Ge source is negligible owing to the exponential decrease in hole concentration with decrease in energy below the Fermi level according to the Fermi-Boltzmann distribution. Thereby, very few holes can flow to the MoS2, leading to a very low OFF-state current. With an gate voltage applied is sufficiently negative, such that the valence band of MoS2 near the dielectric interface is lifted above the conduction band of the Ge source, the electrons start to flow leading to an abrupt increase in BTBT current. However, whenever a midgap trap exists in the Ge and occupied by a hole with adequate thermal energy to overcome the barrier of potential energy $E_t=(E_{C,}\text{source}-EV_{,\text{channel}})$, it can tunnel from source to the MoS2 valence band. The subthresold transmission probability that a hole may tunnel can be expressed as $P_{sub} = \exp\left[-E_t(\frac{1}{kT}+\frac{1}{kT^t})\right]$ where kT^t is the swing of the tail-like trap distribution in the Ge. So the trap assisted BTBT in Ge-MoS$_2$ junction can be computed in similar way as that of I_{on}. The expression for trap assisted BTBT as can be expressed using Landauer's formula as

$$I_{off} = q \int_{E_{V,\text{channel}}}^{E_{C,\text{source}}} P_{sub} T_{BTBT}(E) D_{2,TMD}(E)[f_S(E) - f_D(E)] v_y(E) dE \tag{9}$$

Simplifying the above we obtain the trap assisted BTBT current as

$$I_{off} = \frac{q(2m^*{}_{TMD})^{1/2}}{2\pi} P_{sub} T_{BTBT}(E) \left\{\left[F_{1/2}\left(\frac{E_{C,\text{source}}-E_{FS}}{kT}\right) - F_{1/2}\left(\frac{E_{C,\text{source}}-E_{Fs}-E_t}{kT}\right)\right] - \left[F_{1/2}\left(\frac{E_{C,\text{source}}-E_{FD}}{kT}\right) - F_{1/2}\left(\frac{E_{C,\text{source}}-E_{FD}-E_t}{kT}\right)\right]\right\} \tag{10}$$

The complete expression for both OFF state and ON state may be obtained by combining eq. (6) and (10). Since the traps states are available in the Ge forbidden gap to move to the MoS$_2$ valence band the trap assisted tunneling current is much less due to the low DOS in 3-D Ge relative to 2-D DOS involved in ON-state. This quasi-analytical expression provides the current in both subthresold and super threshold condition as

$$I = \begin{cases} I_{on} & V_{gs} > V_{th} \\ I_{off} & V_{gs} < V_{th} \end{cases} \tag{11}$$

3 RESULTS AND DISCUSSIONS

We verify our developed model with the experimental work done in ref [10]. The typical $I - V$ characteristics of the Ge/MoS$_2$ Tunnel FET at room temperature is shown in Fig. 2 with the parameter values taken as in [10]. A good match is obtained with the experimental curves for various drain bias in the low drain current and small gate bias regimes. At high current small deviation of the characteristics are found, which is possibly due to the scattering effect that may occur during transport in the real device, in contrast to the ballistic transport assumed for developing the model. Thus the model overestimates the drain current for high drain current condition and high gate bias especially at saturation, with little offset values. It may be noted that that for all the drain voltage cases considered, Ge/MoS$_2$ Tunnel FET can overcome the fundamental limitations on SS (60mV per decade at room temperature) in MOSFETs, and SS values below 60mVper decade can be estimated over about four decades of current. From Fig. 2 it is observed that the ON- current is quite high. This is due to the small tunneling barrier width attributed to the thickness of the MoS$_2$ planer structure used for the channel material. The transfer characteristics indicate improved transconductance of the device.

In Fig 3 we show the drain current as a function of both linear and logarithmic scale to estimate the subthresold swing (SS) and a very low value of SS is predicted.

In Fig. 4 the I_d-V_d characterics is plotted as function of various gate voltages on both linear and log scale. From the curves it is found that the OFF sate current is very low due to the presence of van der Waals bonding between the two MoS$_2$ layers and the ON sate current is quite high leading to a high ON-OFF ratio. However the increased ON- current reflects that the gate-to-source capacitance will also be high.

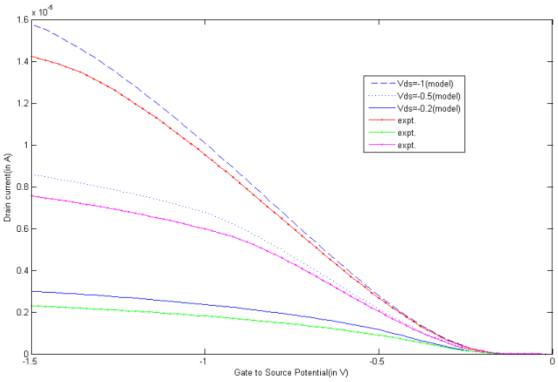

Fig. 2. Modeled and experimental drain current curves (on linear scale) as a function of gate voltage.

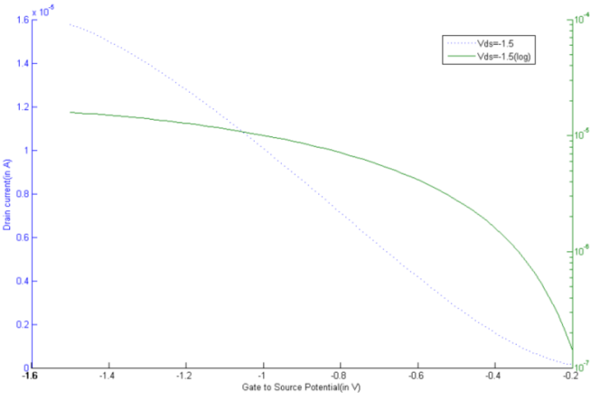

Fig. 3. Modeled drain current (on both linear and log scale) as a function of gate voltage at V_{DS}= -1.5 V.

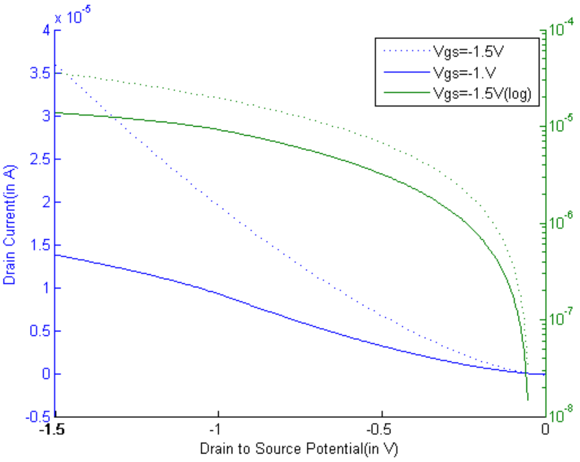

Fig. 4. Modeled drain current (on both log and linear scale) as a function of drain voltage at V_{GS}= -1.5 V and V_{GS}= -1.0 V.

3 CONCLUSION

In conclusion we have developed a compact model suitable for circuit exploration and wide-scale applicability 2-D FET. The I-V characterics provided by the model predicts consideable performance improvements compare to conventional III-V and Si based TFET in terms of current ON-OFF ratio, subthresold swing and gate capacitance. The validity of the proposed model is verified with reported experimental work and good match is obtained.

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