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Design and Implementaion of Energy Efficient 8×8 Multiplier using Single Phase Adiabatic Dynamic Logic

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Abstract: This paper represents the design and implementation of 8x8 adiabatic multiplier using Quasi-Static Single-phase Adiabatic Dynamic Logic (SPADL). SPADL uses only a single sinusoidal supply-clock to for the minimal control circuitry and less power overheads. Simplicity and static logic resembled characteristics of SPADL substantially decreases circuit complexity with improved driving ability and circuit robustness in case of proposed structures. In order to provide insights into difference between the proposed logic and previously reported multiphase logics, 8-bit carry look-ahead adder and multipliers are implemented in TSMC 0.18µm CMOS technology. CADENCE simulations show that SPADL consumes only 61.32% and 51.11% of total energy of the Clocked Adiabatic Logic (CAL) for clock frequencies ranging from 1 MHz to 100 MHz frequency, in case of 8-bit CLA and 8×8 multiplier. SPADL based 8-bit CLA and 8×8 multiplier also save more than 85% energy than the CMOS counterpart at 100 MHz frequency. High energy efficiency of SPADL makes it suitable for implementing performance efficient VLSI circuitry.
Keywords: Adiabatic; energy efficiency; single phase; quasi static; 8x8 Multiplier.

1 INTRODUCTION

Adiabatic circuits achieve low energy dissipation by restricting the current flow across devices with low voltage drop and by recycling the energy stored on their load capacitance by using a time varying AC supply voltage. Several adiabatic logic architectures have been reported [1-7] for low power VLSI design with a single or multiphase clock scheme to steer currents and recycle charges. Implementation of complex control schemes [8, 9] distribution of multiple clock phases [10-12], the management of data dependent clock capacitance fluctuations make the multiphase clocking schemes sensitive to clock skew and may severely limit their high frequency performance [12]. In contrast to multiphase circuits, single-phase adiabatic circuit

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relies on just one phase of a power clock waveform for low power and synchronization. Simply a sinusoidal signal, which can be generated using simple LC circuit with higher energy efficiency, is used as a power clock in a single-phase adiabatic circuit. Due to simple clock scheme, single-phase logic style can enjoy minimal control overheads and are thus capable of operating at high speed, while achieving high-energy efficiency. Motivated by the advantages of single phase clocking recently we have proposed a novel single phase adiabatic dynamic logic (SPADL) [1] that requires only one sinusoidal power clock supply, has simple implementation, and performs better than the previously proposed diode based logic families [6], [7] in terms of energy consumption. SPADL logic features simplicity and static logic resembled characteristics of SPADL substantially decreases transistor overheads and the circuit complexity.

Extensive experiments are done by Cadence Spice spectra in TSMC 0.18μm technology to ensure the high energy efficiency of proposed SPADL logic compared to other imperative multiphase logic styles and also to show that the proposed SPADL logic is feasible for designing of adiabatic circuitry that functions properly at relatively high power clock frequency.

The rest of the paper is organized as follows. Section II describes the operation of SPADL inverter and also addresses the energy dissipation. Implementation of complex circuits like multiplier, experimental results and comparison of performance of our energy recovery logic are also detailed in section III. Finally conclusions are given in section IV.

2 SPADL LOGICS

Rudimentary operations and energy consumptions of SPADL structures are discussed in [1]. Fig. 1(a) and 1 (b) show the configuration of a SPADL block and inverter respectively. Hence only a sinusoidal clock (φ) is used to reduce clocking overheads. Moreover circuit complexity is also reduced greatly due to resemblance with the static CMOS logic.

In SPADL inverter, shown in Fig. 1(b), during discharging when M2 and M5 both NMOS are ON, parallel combination of them reduce effective resistance between V_x and V_n. Also voltage drops (V_o- V_n) across drain and source terminals increase the gate to source voltage swing of M5. Increased gate to source swing reduces the ON resistance of M5. Due to the reduction in ON resistance and low resistive parallel paths, discharging current from output to the supply clock increases, this in turn improves the lower swing significantly in SPADL

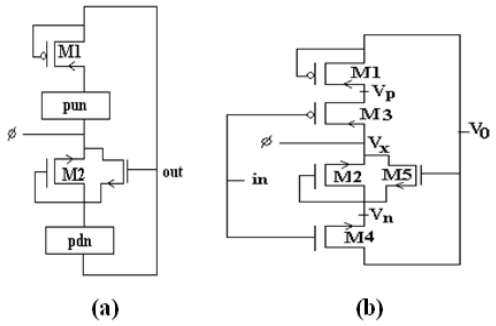

Fig. 1(a). Spadl block (b) spadl inverter.

logic. Hence we get,

$$V(1) = (\varphi|_{max}-|V_{TP}|) \text{ and}$$
$$V(0)=\Delta V \text{ (where } 0<\Delta V<|V_{TN}|) \quad (1)$$

In SPADL total energy dissipation (E_{Ad}) in charging path, becomes:

$$E_{Ad} = E_{Diode} + E_{Tx}$$
$$\approx[C_L|V_{TP}|(V_{DD}-|V_{TP}|)] + [½C_L|V_{TP}|^2] \quad (2)$$

E_{Diode} and E_{Tx} represent the energy dissipation across M1 diode and M3 transistor. During discharging almost same amount of energy dissipates in the discharging path. Assuming that CV_{DD}^2 (= E_{Conv}) energy losses in a conventional CMOS logic circuit, maximum possible energy saving of SPADL logic over CMOS in a full clock cycle is,

$$\eta_{\%} = (E_{Ad}/E_{Conv})\times 100 \approx [\alpha\{1-\alpha\}]\times 100 \quad (3)$$

Where $\alpha = \{|V_{TP}|/V_{DD}\}$. It is seen that there is a bit of improvement in energy efficiencies of SPADL logic by lowering threshold voltage of PMOS and NMOS diode. Still we cannot reduce threshold or supply voltage arbitrarily. As aggressive scaling of technology results in different leakage components become a significant issue of total power dissipation in adiabatic CMOS logic circuit.

3 8X8 SPADL MULTIPLIER

Complex gates can be easily implemented by using simple CMOS pull-up and pull-down network. In Fig. 1(a), by replacing the PUN (pull up network) or PDN (pull down network) we can implement the AND gate, XOR gate, AND-OR and buffer with SPADL circuit topology. Fig. 2 shows implementation of all these gates with simple full adder and buffer circuit. Static logic resembled characteristics of SPADL logic substantially decreases the transistor overheads in complex gate design. Thus Complex gate design becomes very modular and simple.

To demonstrate the extensibility of the SPADL, we have designed 4×4 and 8×8 carry–save multiplier based on the proposed circuit topology. In 8×8 SPADL multiplier, 8-bit carry–look ahead adder is used for addition purpose in the last stage of the multiplier. We chose a CLA structure according to the computational model of Brent and Kung that allows a fast carry computation since the delay to add two numbers depends on the logarithm of the size of the operands: $\Delta \approx \log[N]$ and, there-fore, a reduction of the adder logic depth.

The schematic view of an 8 bit CLA structure by using SPADL is shown in Fig. 3, circles and arrows highlight the fast carry computation tree. In CLA structure AND, OR, XOR and buffers are used mainly. In CLA structure we have designed the AND-OR block in a single stage to get output after a single clock phase, otherwise clock synchronization will be difficult. In Fig. 2 (d) assuming all the inputs are at 'logic 1' ('logic 0'), when Φ ramps up (down), 'out' node will be charged up (discharged) through the NMOS (PMOS) networks and PMOS (NMOS) diode, which gives 'logic 1'('logic 0') at 'out' node. Hence though six stages of gates are used yet instead of 6T we can get the output after 3T (6×T/2=3T) as the output of every stage can be evaluated during every half of the clock periods due to single phase operation. In other words we can drive the high frequency data by low frequency (almost half) clock. So the proposed SPADL CLA has a latency of six clock phases (three clock cycles). Hence, energy recovery techniques are more suitable for some specific applications where speed and latency are critical. However, since each SPADL gate has two more transistors (due to diodes) than the conventional CMOS gate, the transistor overhead decreases substantially in case of CLA structure. In addition, single-phase sinusoidal supply clock ensures lower energy dissipation, and also simplifies the clock tree design. The proposed approach not only eliminates the intolerable delay but also reduces the routing complexity also. In case of 8-bit CLA energy comparison per cycle in between SPADL, CAL, 2N2N2P2D, PFAL and static CMOS are shown in Fig. 4.

In 8×8 multiplier circuit, a simple adder block shown in Fig. 2(e), is used as the basic building block. Fig. 5 shows the organization of the SPADL multiplier, which is identical to conventional CMOS carry–save multiplier. $X=\{X_0, X_1, \ldots, X_7\}$ and $Y=\{Y_0, Y_1, \ldots, Y_7\}$ are the inputs and $Z=\{Z_0, Z_1, \ldots\ldots, Z_{15}\}$ is the output. A counting sequence $X=\{X_0, X_1, \ldots, X_7\}$ =00000001, 00000010,. …., 11111111 and $Y=\{Y_0, Y_1, \ldots, Y_7\}$ = 00000100 are assigned as the test patterns, in case of CLA. As we simulate the bench for roughly 56 cycles, the output results are $Z=\{Z_0, Z_1, \ldots\ldots, Z_{15}\}$ = 00…000100, 00..001000, 00..001100, 00..0010000, . . , 0000000011110000. Waveform of 8×8 SPADL multiplier is shown in Fig. 8.

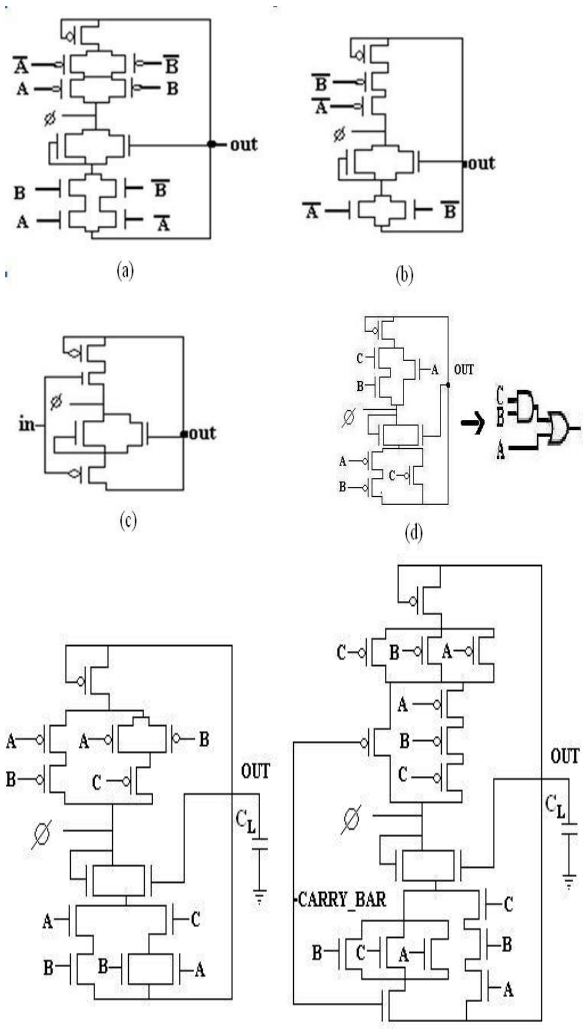

Fig. 2. Spadl gates (a) xor (b) and (c) buffer (d) and-or (e) spadl adder.

Hence both of the CLA and multiplier circuits of SPADL, along with other imperative logic styles like CAL, 2N2N2P2D, PFAL and static CMOS have been simulated. As comparison parameter we use the adiabatic gain (G), where Adiabatic Gain = the ratio between the power consumption per cycle by static CMOS logic and SPADL logic. So percentage of power savings by SPADL logic can be calculated by η (%) = {1-(1/G)}×100. Also the adiabatic gain (G) comparison of different adiabatic arithmetic circuits, including 4-bit CLA, 8-bit CLA, 4×4 multiplier and 8×8 multipliers are shown in Fig. 7. Fig. 8 show the energy consumption per cycle in case of 8×8 multiplier for different

adiabatic logics like CAL, 2N2N2P2D, SPADL and conventional CMOS.

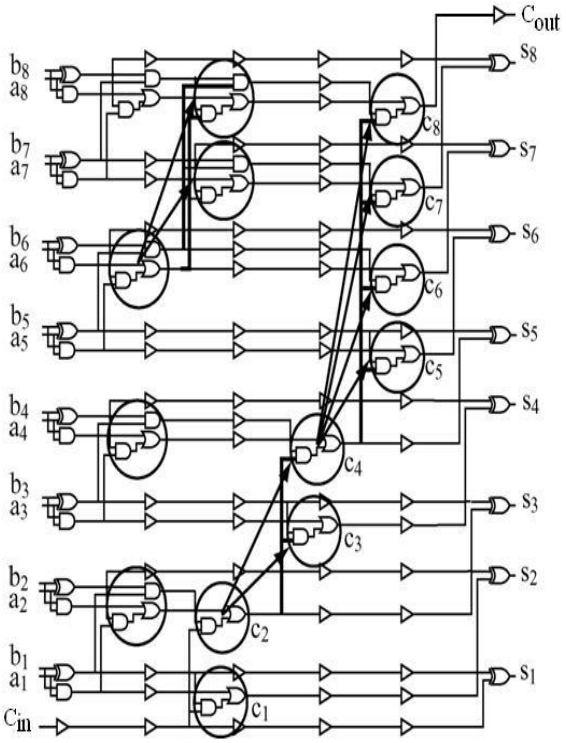

Fig. 3. Schematic of 8 bit spadl carry look ahead adder.

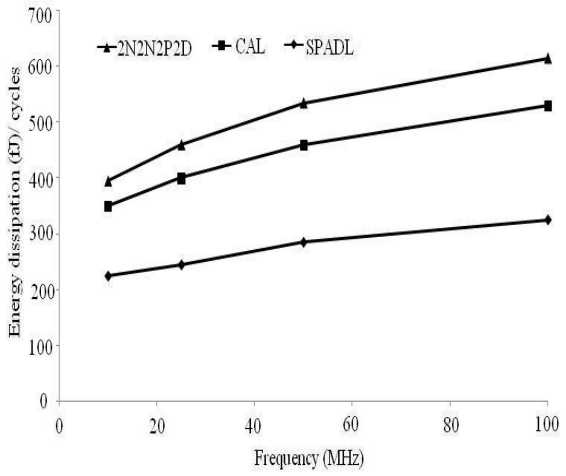

Fig. 4. Comparison of energy consumption per cycle for different 8 bit adiabatic clas with frequency variation.

We use the SPADL buffer, shown in Fig. 2(c) at the output of every final stage. These extra nodes can contribute a significant amount of power dissipation depending on how often they are used in the circuits. To improve noise immunity, extra power dissipation from these circuits mayoffset the gains in more widespread circuit applications by the energy-recovery logic. From Fig. 7 and Fig. 8, we find that though adiabatic gain (G) at 1MHz in case of 8 bit CLA and 8×8 multiplier circuit are 63% and 25%, yet at 100 MHz these "G" become 35% and 7.5%. If we move at higher frequency regime (≈ 100MHz) then the "diode transistors" need to be sized up proportionately, which increases the capacitances. The resistive dissipation (which is proportional to RC/T) increases as well. At low frequency, the energy consumption of SPADL circuits is mainly due to the threshold loss, independent of frequency. For SPADL circuits, low-threshold diodes will be needed for higher energy efficiency and high swing. Devices optimized for low diffusion capacitances and coupling capacitances are desired for better noise immunity.

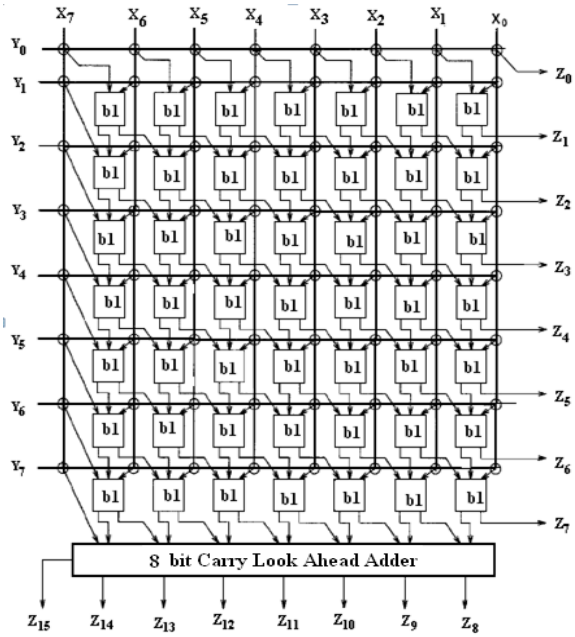

Fig. 5. Schematic of 8x8 spadl multiplier.

At low frequency, all single phase logic styles (CAL and SPADL) promise substantial energy savings compared to static CMOS, with the lowest energy consumption from SPADL. SPADL based 8-bit CLA consumes only 34.10 % and 49.24 % of total energy consumed by conventional 8 bit CLA at 10 MHz and 100 MHz frequencies respectively. As the latches are introduced at the end of 3 stages in 8 bit CLA circuit to improve the driving ability, some extra power dissipates at 100 MHz frequency. Still at 100 MHz frequency, SPADL logic based CLA consumes only 61.32 % and 52.84 % energy of the CAL and 2N2N2P2D based 8 bit CLA respectively. In case of 8×8 multiplier circuit, neither the adiabatic CAL and 2N2N2P2D nor the static CMOS logic performs better than SPADL across the entire frequency range of our simulations. In spite of buffers, SPADL multiplier circuit has the least power consumption as compared to CAL, 2N2N2P2D and static CMOS. Compared to the CAL and 2N2N2P2D, at high frequency regime

like 100 MHz, though SPADL 8×8 multiplier consumes only 51.11% and 43% of total energy, respectively.

Adiabatic arithmetic units, based on 2N2N2P2D logic do not show much power savings since 2N2N2P2D logic circuit has floating output node during part of the clock cycle. This circuit can only work well if there is substantial capacitance to ground. Otherwise, capacitive coupling between the floating output node and clock would cause inadequate operating margins, which is undesirable as the output is directly connected to the input of the next stage logic in 2N2N2P2D. Moreover implementation of complex triangular waveforms, clock distributions and managements impose limitations at high frequency operation in case of 2N2N2P2D logic. The CAL based CLA, which is geared for very energy efficient operation at very low frequencies (< 1 MHz), is more dissipative than SPADL even at 10 MHz and energy consumption increases with the frequency rapidly. CAL's dynamic nature leads to high switching activity, deteriorate the energy efficiency. So CAL logic is impractical for high-frequency applications. So CAL logic is impractical for high-frequency applications.

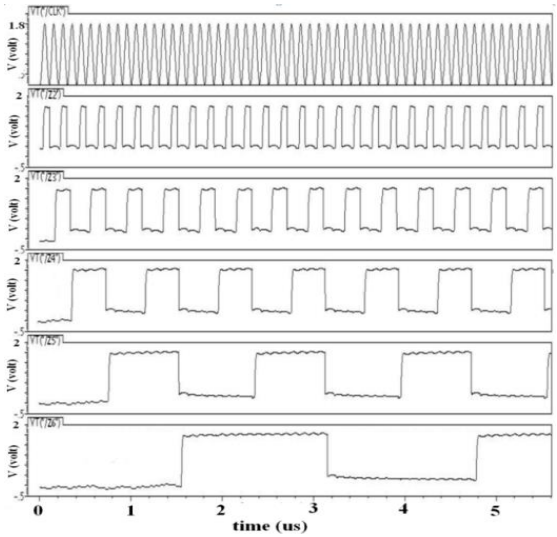

Fig. 6. Output waveforms of 8×8 spadl multiplier.

Also, it should be mentioned that SPADL's most attractive advantage compared to CAL is that its high speed and SPADL cascaded circuits need only one power-clock without any auxiliary timing control voltages. While the CAL takes two periods of charging and discharging, SPADL only needs single period. This ensures less power dissipation for SPADL. Moreover implementation and distribution of auxiliary clocks need extra control circuitry, which also deteriorate the energy efficiencies of CAL at high frequencies.

Nevertheless, SPADL may consume extra power when the input frequency goes low, since the floating nodes are subject to the noises. Therefore, it is believed that SPADL is better used for high frequency applications.

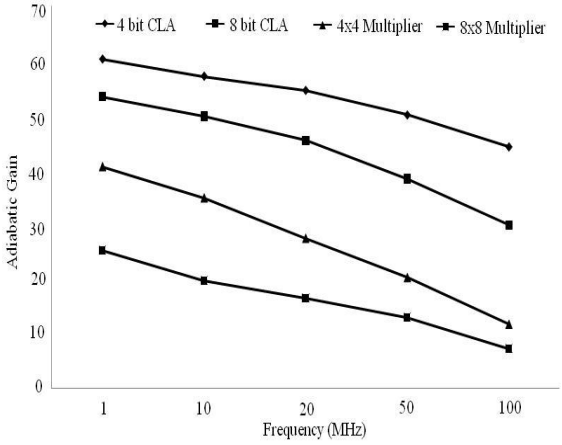

Fig 7. Gain comparison of different adiabatic arithmetic units.

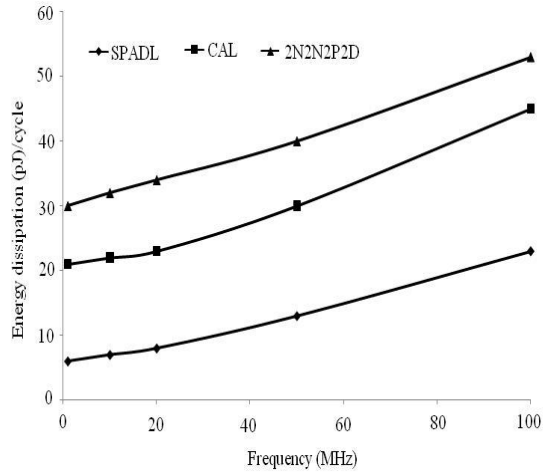

Fig. 8. Comparison of energy consumption per cycle for different adiabatic 8x8 multipliers.

4 CONCLUSION

In this paper, we have presented a quasi-static adiabatic approach by using a single phase ac supply. The total energy consumption of the proposed SPADL logic is significantly reduced, because the energy transferred to power clock is mostly recovered by using low resistive parallel path from output node to the supply clock. In addition to the summary of previous works, we analyzed SPADL in detail, and elaborated relative strength and weaknesses. Both simulations and measurement results verify the functionality of such logic, making it suitable for implementing energy-aware and performance- efficient very-large scale integration (VLSI) circuitry.

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