Area Efficient Low Power Scan Flip-Flop Design Based on Quantum-Dot Cellular Automata

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Abstract: Minute digital circuit at nanoscale can be designed using Quantum-Dot Cellular Automata (QCA). Due to inherent nature, QCA circuits have low power dissipation and can perform faster switching during operations. This work illustrates a new QCA based design of 2:1 multiplexer and D flip-flop. Farther those designs are used to achieve an optimized circuit for scan flip-flop. The designs are claimed optimized after comparing with existing ones in the start of the art. Design accuracy is confirmed with theoretical values. The estimation of power dissipation is achieved, which shows the circuits have low power dissipation. The designs can be used to as a building block to achieve low power general purpose nano-processor.

Keywords: QCA; majority gate; multiplexer; D flip-flop; scan flip-flop; power dissipation.

1 INTRODUCTION

A revolution has been started off in the field of nano digital circuits [1-5] as well as nano communication [6-10] using QCA. This is one of the upcoming technologies which have left behind CMOS technology in terms of density of the circuits, their functional capacity as well as power consumption [1, 6-12]. Power consumption is actually very low since QCA does not require any electricity from external source [13-16]. Based on the arrangement of electrons within the quantum dot cells gives rise to electrostatic charge, this combined with columbic effect gives rise to two stable states when two or more QCA cells are placed side by side. The bi-stable nature of the circuit is used for doing any type of computations in digital field [15-20]. Another added advantage of QCA circuits is that they perform their functionalities at a very high clock frequency.

A novel circuit of the 2:1 multiplexer (MUX), D flip-flop and scan flip-flop has been designed. In this paper more importance is given to reduce the size and latency of the proposed circuits to minimize its energy consumption.

The contributions of this work are as follows.

(1) New layout design for 2:1 multiplexer (MUX), D flip-flop and scan flip-flop.

(2) Comparison with existing layouts to establish the advancement of the proposed layouts in terms of area and latency.

ISSN: 2222-7059 (print), ISSN: 2222-7067 (online), http://www.aspbs.com/aiem
DOI: 10.7508/aiem.2016.01.030

(3) Estimation of power dissipation by the layouts.

(4) Testing of design accuracy.

The paper is organized as follows. In section 2, overview of QCA devices and QCA clocking technique are explored. Section 3 deals with design of proposed work. In section 4, simulation results, circuit complexity, comparison with existing layouts and estimation of power dissipation have been illustrated. Finally in section 5, conclusion has been drawn.

2 QCA OVERVIEW

2.1 Basic QCA Devices

As shown in the Fig. 1a, four quantum dots are present at the four corners of a QCA cell but electrons are present only within two dots, which are diagonal to each other [21-24]. The electrons can move between the adjacent cells with the help tunnels present within these dots. These two electrons within the quantum cells give rise to two different polarities '1' and '0'. It is represented by P_l as revealed in the Fig. 1. P_l = + 1 and P_l =-1 represents binary value '1' and binary value '0' respectively stored within the QCA cell. An un-polarized cell can be recognized when the value of P_l = 0, this convey the idea that no information is present within the QCA cell [24, 25]. But these structures are not fixed. They can be interchanged.

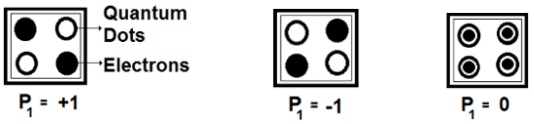
When more than one QCA cells are placed adjacent to each other a columbic effect will be raised between the electrons due to harmonization of adjoining cells, which must give rise to alteration in the polarization of the adjacent cells [5-7]. With QCA cells, primary logic gates can be implemented easily. They are termed as majority a gate which is constituted of five cells, having three inputs, a single intermediately cell and one output as depicted in Fig. 2(a) and also its QCA layout depicted in Fig. 2(b). In majority gate as their name conveys "majority" means its output will be based on the dominance of the values given as inputs [8-11, 27]. If X, Y, Z are the inputs to a majority gate, and its matching logical expression can be written as

$$M(X, Y, Z) = XY + YZ + XZ \quad (1)$$

When one of these three inputs of the majority gate is fixed to logic value '0' then logic AND-gate is created and when it is fixed to logic value '1', then logic OR gate is created [3-4]. Both of them are shown in Fig. 3 and written as

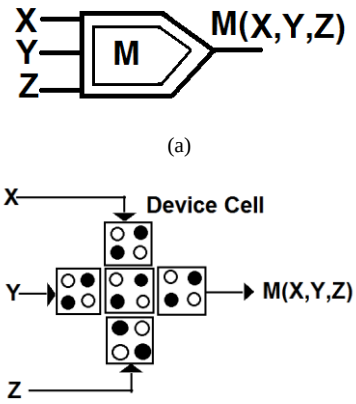
$$M(X, Y, 0) = X.Y \quad (2)$$

$$M(X, Y, 1) = X + Y \quad (3)$$



(a) (b) (c)

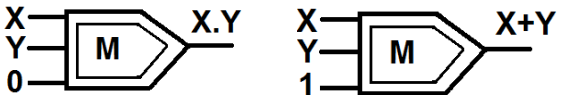
Fig. 1. Different structure of QCA cell. (a) Binary '1', (b) Binary '0', and (c) No information.



(a)

(b)

Fig. 2. QCA majority gate. (a) Block Diagram, (b) QCA layout.



(a) (b)

Fig. 3. Majority gate acting as (a) AND-Gate, (b) OR-Gate.

2.2 QCA Clock

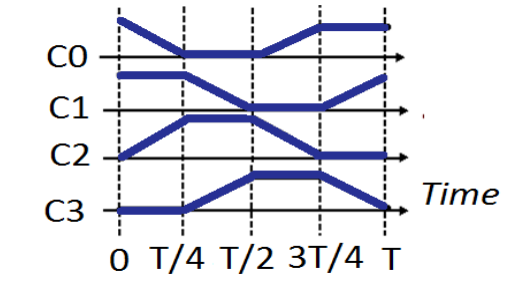
Clock is one of the important features to control CMOS circuits. Similarly QCA circuit is also controlled by clock [1-5]. In order to control the potential barrier which exists when the electrons present in the quantum dots as they try to move along the tunnel junction and another barrier comes into play when switching occurs between the cells. In order to synchronize the flow of information, clocks are necessary. Four different clocking zones are present in QCA clocking as shown in Fig. 4. Each of the clock signal phase are lagged by $\pi/2$ degrees. The four phases are switch phase, hold phase, release phase and relax phase respectively.

1) Switch phase- This phase give rise to polarization. Here initial starts of tunneling of electrons are held strongly due to obstruction caused by the polarization effect between the dots.

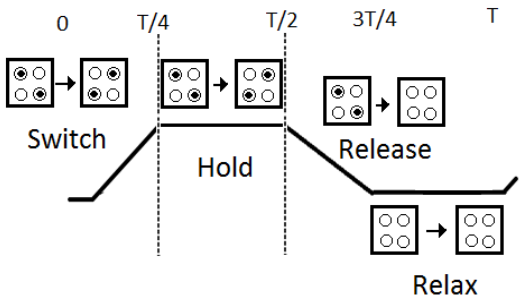
2) Hold phase- As the name of this phase depicts the electrons will be strongly held in their previous position within the cell as polarization remains same as achieved in the last phase.

3) Release phase- In this phase QCA cell's polarization is lost and it is converted back into its normal un-polarized state. As a result the obstruction between dots is reduced and the electrons can move through dots.

4) *Relax phase–* The obstruction between the quantum dots remain as same as obtained in the release phase and therefore the cell's state remains same.



(a)



(b)

Fig. 4. QCA clocking. (a) Four phase, (b) Operation in single cycle.

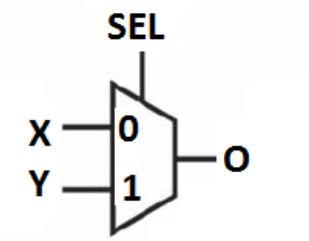
3 PROPOSED WORK

In this section, proposed design of scan flip-flop is described. To design the scan flip-flop, first 2:1 multiplexer and D flip-flop are designed in QCA. Then cascading those circuits, the layout of scan flip-flop has been achieved.

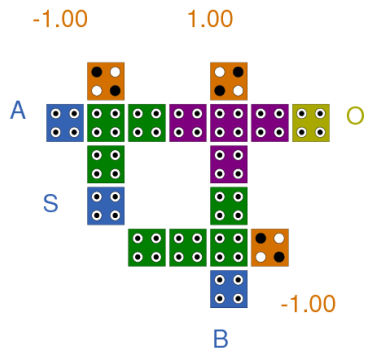
3.1 2:1 Multiplexer

One of the basic combinational circuits is a multiplexer. It consists of n input lines, m select input lines and one output line. The output will depend on one of the inputs selected by the select input lines. During communication of analog or digital signals, multiplexers are considered for selecting and transmitting signals at a high speed on different communication channels. There are different types of multiplexers. Basic among them is the 2:1 multiplexer (MUX), which consists of two input lines and one select line required to select anyone of the inputs as output [28, 29]. The block diagram of the 2:1 MUX is given in Fig. 5a. X, Y stands for the inputs, SEL represents the control input and O is the output bit. The logic equation is shown in equation (4). The corresponding QCA layout is shown in Fig. 5b. This layout is composed of three majority voters (MVs), one inverter and three clocking zones.

$$O=X.(SEL)´+Y.(SEL) \quad (4)$$



(a)

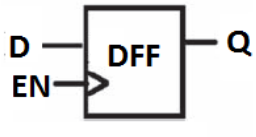


(b)

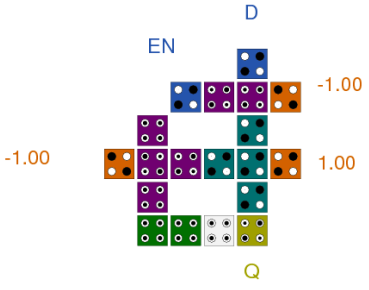
Fig. 5. Proposed 2:1 mux. (a) Block diagram, (b) QCA layout.

3.2 D Flip-Flop

D flip-flop is the revised form of R-S flip-flop having an inverter at position R [30-32]. The block diagram is shown in Fig. 6a. Thus, the amount of inputs reduces to one. The characteristic equation



(a)



(b)

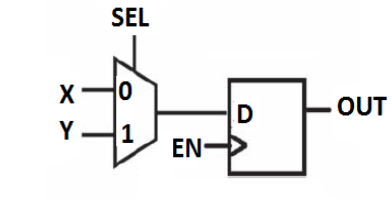
Fig. 6. Proposed D flip-flop. (a) Block diagram, (b) QCA layout.

for D flip-flop is in equation (5). The QCA layout corresponding to Fig. 6a is shown in Fig. 6b. The layout is composed of three MVs, one inverter and four clocking zones.

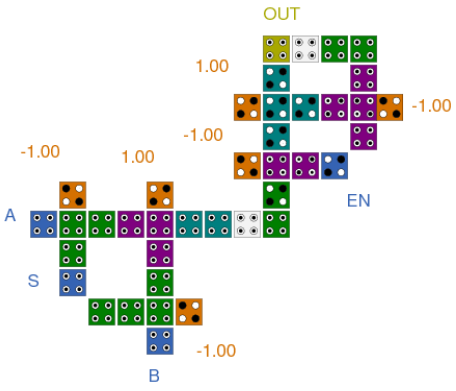
$$Q(t+1) = D \quad (5)$$

3.3 Scan Flip-Flop

Fig. 7a shows the block diagram of scan flip-flop. It is made by cascading one 2:1 MUX with one D flip-flop [33]. The control bit SEL is responsible for selecting the signal to perform either normal operation or scan operation. The output signal from the MUX is applied as an input signal to the D flip-flop. OUT represents the final output value. EN is the enable input signal for the D flip-flop. The equivalent QCA layout for proposed scan flip-flop is shown in Fig. 7b. The layout is composed of six MVs, two inverter and eight clocking zones.



(a)



(b)

Fig. 7. Proposed scan flip-flop. (a) Block diagram, (b) QCA layout.

4 RESULT AND DISSCUSSIONS

4.1 Simulation Results

All the designs are designed and simulated using QCADesigner tool [27]. The simulation results are shown through Fig. 8 to Fig. 10. All the designs are tested against theoretical values. This testing is performed to achieve accurate design for the proposed circuits.

4.2 Design Complexity

In order to implement the proposed 2:1 MUX, three MVs and one inverter are required. Besides, 18 quantum dot cells are required which occupies a total area of 0.017 μm^2 whereas its cell area is 0.007 μm^2. The calculated area of usage is 41.17 %. Similarly, for D flip-flop and scan flip-flop the complexities are shown in Table 1.

4.3 Comparison with Existing Layouts

Table 2 shows a comparison between the proposed multiplexer design and existing multiplexer circuits. It has been observed that improvement in terms of

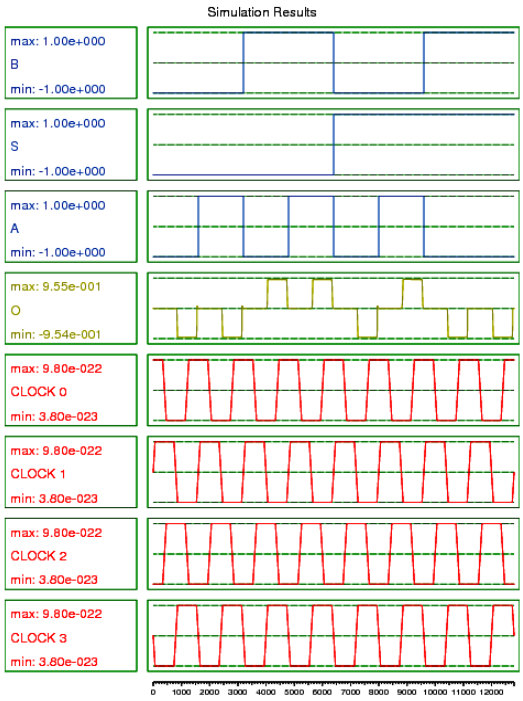


Fig. 8. Simulation result of proposed 2:1 mux.

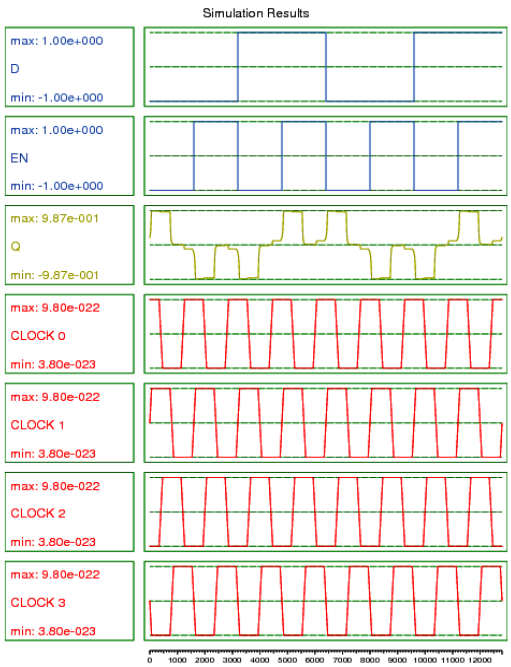


Fig. 9. Simulation result of proposed d flip-flop.

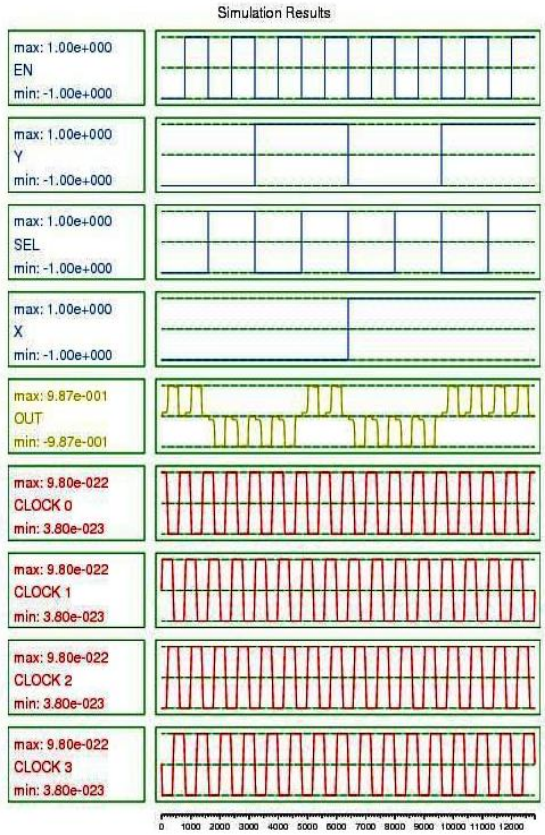


Fig. 10. Simulation result of proposed scan flip-flop.

cell count, the proposed circuit is 68.42% better than existing work [28] and 33.33% better than the existing layouts [29] and again for area of usage the proposed circuit is 15.84% better than over [28] and 3.67% better than over the layout at shown in [29].

Table 3 shows a comparison between the proposed D flip-flop design and existing D flip-flop circuits. It has been observed that improvement in terms of cell count the proposed circuit is 45.71%, 72.06% and 54.06% better than the existing layouts [30-32], respectively and in terms of area of usage is considered, the proposed circuit is 5.30%, 17.45% and 19.97 % is better than layouts [30-32], respectively.

The comparison between the proposed scan flip-flop design and existing scan flip-flop circuits is shown in Table 4. It has been observed that improvement in terms of cell count the proposed circuit is 54.44% better than the existing [33] layout and in terms of area of usage is considered, the proposed circuit is 7.73% better than existing [33] layout.

4.4 Power Dissipation by of Proposed Layouts

In QCA circuit, the power dissipated by each cell is

Table 1. Complexity of proposed designs.

QCA Circuit	No. of MVs and Inverters	Cell Count	Total Area (μm^2)	Cell Area (μm^2)	Area Usages (%)
2:1 MUX	3 MVs and 1 inverter	18	0.017	0.007	41.17
D flip-flop	3 MVs and 1 inverter	19	0.014	0.008	57.15
Scan flip-flop	6 MVs and 2 inverter	41	0.06	0.016	26.67

Table 2. Proposed 2:1 MUX vs existing layouts.

QCA based 2:1 MUX	Cell count	Total area (μm^2)	Cell area (μm^2)	Area usages (%)
Proposed layout	18	0.017	0.007	41.17
Existing [28]	57	0.073	0.019	25.33
Improvements (%)	68.42	76.71	63.16	15.84
Existing [29]	27	0.233	0.088	37.50
Improvements (%)	33.33	92.70	92.05	3.67

Table 3. Proposed D flip-flop vs existing layouts.

QCA based D flip-flop	Cell Count	Total Area (μm^2)	Cell Area (μm^2)	Area Usages (%)
Proposed layout	19	0.014	0.008	57.15
Existing [30]	35	0.027	0.014	51.85
Improvements (%)	45.71	48.14	42.8	5.30
Existing [31]	68	0.068	0.027	39.70
Improvements (%)	72.06	79.41	70.37	17.45
Existing [32]	42	0.045	0.017	37.78
Improvements (%)	54.76	68.89	52.94	19.97

Table 4. Proposed scan flip-flop vs existing layout.

QCA based scan flip-flop	Cell Count	Total Area (μm^2)	Cell Area (μm^2)	Area Usages (%)
Proposed layout	41	0.06	0.016	26.67
Existing [33]	90	0.19	0.036	18.94
Improvements (%)	54.44	68.42	62.50	7.73

equivalent. The power dissipation of any QCA architecture is the sum of total power dissipated by individual majority gates and the total power dissipated by individual inverters [34]. In this paper, Hamming distance based procedure reported in the work [34] has been employed to estimate the dissipated power. The calculation is performed considering the elevated tunnelling energy level. The outcome is shown in Table 5. For better visualization, the result is also plotted through Fig. 11. During calculation, the temperature (T)=2K has been considered. Here, E_k represents kink energy. γ is for tunneling energy and K is for Kelvin.

Table 5. Dissipated power by the layouts.

Tunneling Energy (γ)	**Power Dissipation (meV)**		
	2:1 multiplexer	***D flip-flop***	***Scan flip-flop***
0.25E_k	104.3	104.3	208.6
0.50E_k	107.8	107.8	215.6
0.75E_k	113.3	113.0	226.6
1.00E_k	119.6	116.6	239.2

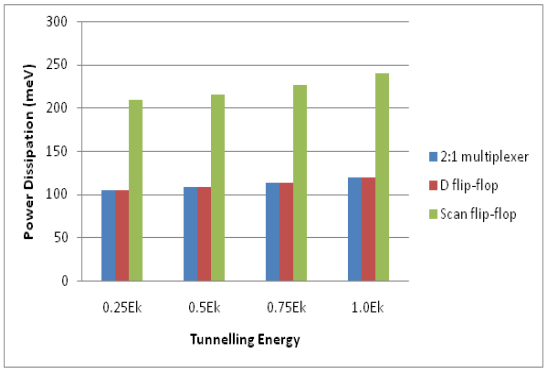


Fig. 11. Power dissipation at different energy levels.

5 CONCLUSION

In this paper more compact form of circuits for 2:1 MUX, D-flip-flop and scan flip-flop are achieved and compared to the existing layouts. Another important feature of the circuits is that the number cell count and clock cycle requirement are lower than existing layouts. Estimation of power dissipation shows that the circuits have low power dissipation. These simpler circuits are useful to produce more complex circuits such as router, shift register at nano scale having low power dissipation.

ACKNOWLEDGMENTS

The authors are grateful to The University Grants Commission, India, for providing with the grant for accomplishment of the project under the UGC Major Project File No. 41-631/2012(SR).

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