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Analog/RF performance and Linearity Investigation of Si-based Double Gate Tunnel FET

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Abstract: In this paper, we present a simulation study to report the effect of gate-length downscaling on the analog/RF performance and Linearity investigation of Si-based DG Tunnel FET (TFET). The different RF/analog figure-of-merits such as g_m, R_O, intrinsic gain, f_T, f_{max} and GBW and 1-dB Compression point considered as important linearity matrices of a TFET are extracted and the influence of gate-length downscaling on these parameters is analyzed. Results reveals that superior RF and Linearity performance was obtained with gate-length downscaling. However, these advantages diminishes in terms of poor analog performance with gate-length downscaling. This clearly indicates a trade-off between the analog and RF performance of a down-scaled Si-based TFET. This paper concludes that Si-based TFETs have enormous potential to be a promising contender to the conventional bulk MOSFETs for realization of future generation low-power analog/RF applications.

Keywords: Tunnel FET; transconductance; transconductance generation factor; cut-off frequency; maximum frequency of oscillation; gain bandwidth product; TCAD; 1-dB compression point.

1 INTRODUCTION

The design of most ICs is nowadays constrained by the budget of dissipated power. The energy efficient ICs expected to be working with a V_{DD} less than 0.5V [1], need a steep sub threshold swing. For a conventional bulk MOSFET, the best possible sub threshold swing (SS) is limited (60mv/dec). This fixed slope means, if we want to shift V_T by 60 mV, then the price to pay is an increase of one decade of off-current and in turn of static power. In this respect, International Technology Roadmap for Semiconductors (ITRS) [2] has specified Tunnel FET (TFET) as most promising solution for obtaining Steep Sub-threshold swing [3]. When a Tunnel FET is OFF, only p-i-n diode leakage current flows between the source and drain, and this current can be extremely low (less than a fA/µm). But, when a positive voltage is applied to the gate, on the other hand, the energy bands in the intrinsic region are pushed down and tunneling takes place

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between the valence band of the p^+-region and the conduction band of the intrinsic region. The energy barrier width for band-to-band tunneling is the single most important factor that determines the amount of drain current through a Tunnel. There has been FET [4]. Experimental demonstration of TFET offering SS less than 60mv/dec. A multi-gate TFET offers the additional advantage of better electrostatic control [5] to improve the ON-current and sub-threshold swing. On the other hand, Si-based TFET has significant shown improvement in On-state current due to their low effective mass, small effective tunneling barrier width and low band gap [6]. In this study, we have chosen Si-based TFET to combine the superior electrostatic control of structure for higher scalability and benefit from the material properties of Si. Recently, MOS technology has become a serious contender for RF and analog applications which was previously dominated by the bipolar technologies with the recent trend to reuse the mainstream digital CMOS technologies for analog/RF applications [7]. Therefore, it is important to study the RF/analog performance of devices optimized for digital circuits for possible use in analog/mixed-mode circuits within a SoC. As a result, a deeper understanding of scaling effects on RF/analog performance parameter is crucial. Therefore, for a scaled Si-based TFET, RF device modeling and parameter extraction is not only important for proper understanding of the characteristics of the device but also a prerequisite to design the ICs for RF/analog application [8-9]. The RF/analog performance investigation of Si-based TFETs is still largely unexplored except a few reported [10-11]. This paper presents a simulation study exploring the RF and analog performance parameter investigation of Si-based TFET for use in system-on-chip (SoC) applications. Linearity performance is still an unexplored area and needs to be investigated too. Therefore, in this work, we focus on studying the linearity performance of Si-based TFET to determine their suitability for analog/RF applications. In his paper, our basic aim is to provide more insights related to the effect of gate-length downscaling on the analog/RF behavior of Si-based TFET. This paper is organized as follows. Section II demonstrates the device structure and the simulation setup. In section, III, Results and discussions with the variation of analog performance figure-of-merits with gate-length downscaling is provided. Section IV discusses the effect of gate length downscaling on RF performance figure-of-merits. In section V, we discuss the linearity performance of Si-based TFET devices by investigating the trend of variation of 1-dB compression point. In section VI, we draw the conclusions.

2 DEVICE STRUCTURE AND SIMULATION SET-UP

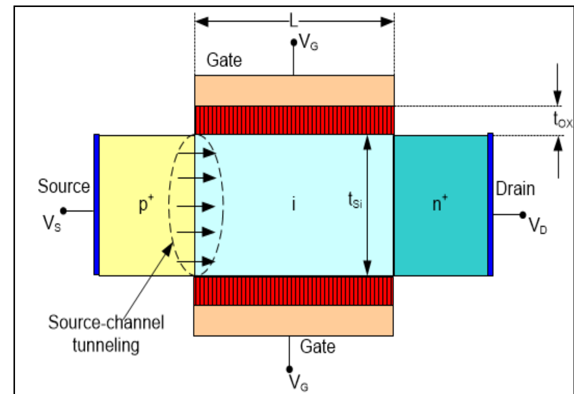

Fig. 1. 2-D cross-sectional structure of Si-based TFET.

Fig. 1 shows the 2-D cross-sectional structure of a Si-based tunnel FET (TFET).The TFET considered in this study uses a P-type Si with doping concentration $N_A = 5X10^{19}$ cm^{-3} as source material, an intrinsic Si channel and a n^+ type Si drain with doping concentration $N_D = 5x10^{18}$ cm^{-3} throughout this work we have used gate insulator with thickness $t_{OX} = 3$ nm (high-k oxide HfO_2 as oxide material) and thickness of body $t_{Si} = 10$ nm, unless otherwise mentioned. Au/Ni is used to create source and drain contact. p^+ poly-silicon with thickness 20 nm is used to form gate contact. Numerical TCAD device simulator SILVACOATLAS [12] has been employed to carry out 2-D simulation of the TFET shown in Fig. 1. Fermi-Dirac carrier statistics along with drift-diffusion (DD) model has been adopted to model the carrier transport. In order to take care of the field assistant mobility Lombard's mobility models has been chosen augmented with concentration dependent mobility models (CONMOB) has been employed to model mobility reduction appearing due to large Concentration gradients. A non local band-to-band tunneling model (BTBT.NONLOCAL) has been employed to model to quantum mechanical tunneling in the TFET considered in this work Shockley-Read-Hall (SRH) recombination method has been used to model recombination characteristics. Newton's method associated with Gummel's numerical technique is used to obtained numerical solution of the differential equation in ATLAS.

3 RESULTS AND DISCUSSION

In order to verify the correctness of the simulation, the transfer characteristics obtained from our simulation is fitted with the results obtained by Pala et al. [13]. In order to achieve the fit, model parameters of CVT mobility model, A and B parameters of the non-local BTBT model along with interface trapped charge density ($D_{it} = 3$ x 10^{12}

states/cm^{2}eV uniformly distributed at semiconductor-oxide interface) is used as a fitting parameters. They are adjusted (BB.A = 5x10^{17} eV^{-2}*s^{-1}*cm^{-1} and BB.B = 2 x 10^6 V/cm) to obtain a nice agreement between our simulated results and results published by Pala et al. [13]. Once the calibration is achieved, the models parameters are used for analysis and extraction of analog/RF performance parameters of Si-based TFET device.

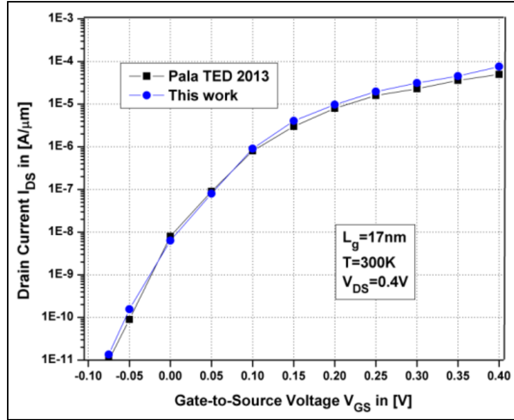

Fig. 2. Simulator calibration by fitting our simulated transfer characteristics with a recent published result by Pala et al. [13] with similar device dimension and structure.

Fig. 3 plots the variation of drain current as a function of drain current as a function of V_{GS} for different channel length. It is evident from Fig. 3 that it decreases in the channel length results in higher ON-state current but at the cost of higher OFF-state leakage current I_{OFF}.

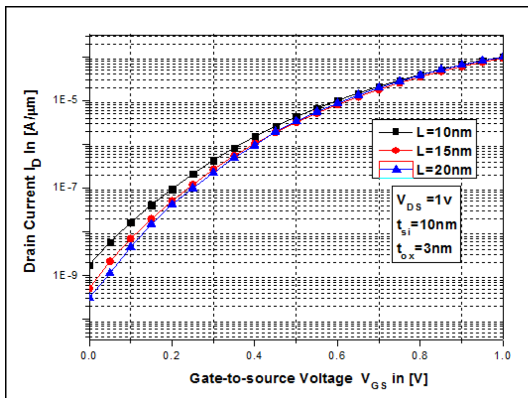

Fig. 3. Variation of Drain Current I_D as a function of Gate-to-source voltage V_{GS} for different channel lengths L=10nm, 15nm, 20nm with device parameter values V_{DS} = 1 v, t_{Si} = 10 nm and t_{OX} = 3 nm.

3.1 Analog Performance Investigation

Transconductance plays a major role in the design of analog circuits such as operational amplifiers (OP-AMPs) and operational transconductance amplifiers (OTAs) having an effect on DC gain, bandwidth, noise performance and offset. Fig. 4 shows the variation of transconductance g_m as a function of V_{GS} for different channel lengths. Due to excellent sub threshold swing of TFET devices, a high value of transconductance is achieved from a Si-based TFET device. Fig. 4 reveals that a decrease in drain current causes decreases in the g_m.

Fig. 5 shows the variation of transconductance generation factor (TGF) as a function of V_{GS} for two different channel lengths. A higher TGF indicates the amplification delivered by the device per unit drain current to obtain that amplification. Our aim is to increase (TGF) so that it can be employed for the realization of low power & high gain analog circuits. However, it is worth mentioning that high (TGF) are suffers with problems associated with linearity.

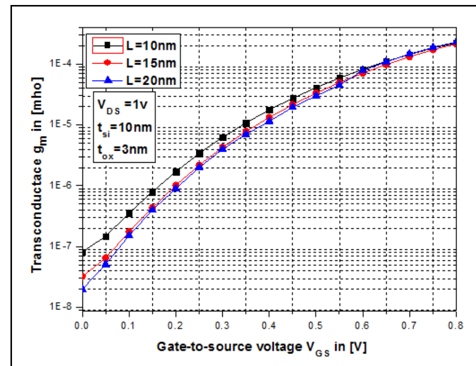

Fig. 4. Plot of variation of transconductance (g_m) as a function of Gate-to-source voltage V_{GS} for different Channel lengths L = 10 nm, 15 nm, 20 nm with device parameter values V_{DS} = 1 v, t_{Si} = 10 nm and t_{OX} = 3 nm.

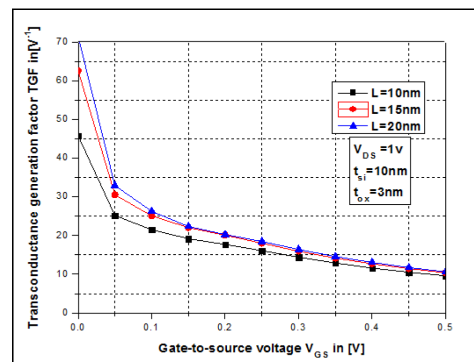

Fig. 5. Variation of Transconductance Generation Factor (TGF) as a function of Gate-to-source voltage V_{GS} for different Channel lengths L = 10 nm, 15 nm, 20 nm with device parameter values V_{DS} = 1 v, t_{Si} = 10 nm and t_{OX} = 3 nm.

The linearity issues of a Si-based TFET device are discussed in section-V of this paper. It is worth mentioning that since sub threshold current in a MOSFET follows kT/q slope, the maximum TGF obtained from a MOSFET is limited to 38V^{-1}. However, for Si-based TFET devices, due to

excellent sub threshold swing higher TGF can be achieved especially for low current densities (small gate bias).

This indicates the applicability of a Si-based TFET device for low-power analog/RF applications. Moreover, Fig. 5 also reveals that as gate length increases TGF increases.

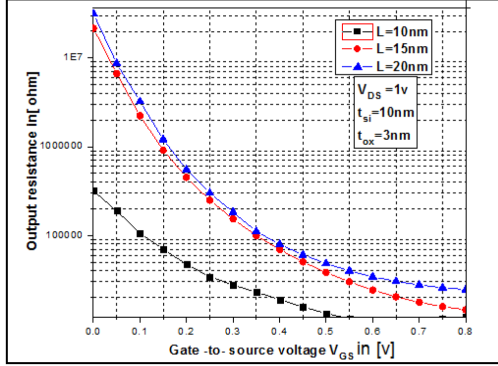

Fig.6: Variation of Output Resistance (R_O) as a function of Gate-to-source voltage (V_{GS}) for different Channel Lengths L = 10 nm, 15 nm, 20 nm with device parameter values V_{DS} = 1 v, t_{Si} = 10 nm and t_{OX} = 3 nm.

Fig. 6 plots the variation of output resistance for different channel lengths. TFET exhibits an excellent current saturation behaviour with negligible channel-length modulation (CLM) [4], thus resulting in a higher output resistance as compared to a conventional MOSFET. This result is consistent with the earlier published results [15-16]. A higher output resistance indicates good current saturation which may be employed in order to obtain a higher intrinsic gain. Fig. 6 indicates that output resistance decreases as channel length decreases. Therefore, it may be concluded that the analog performance of Si-based TFET suffers with gate- length downscaling.

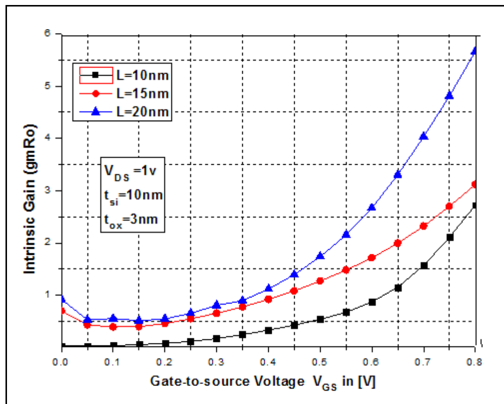

Fig. 7. Variation of Intrinsic gain (g_mR_O) as a function of V_{GS} for different Channel Length L = 10 nm, 15 nm, 20 nm with device parameter values V_{DS} = 1 v, t_{Si} = 10 nm and t_{OX} = 3 nm.

Fig. 7 shows the intrinsic gain defined as the product of transconductance and output resistance (g_m*R_O) as a function of V_{GS}. A lower value of device gain is obtained from a downscaled device; therefore in general we may conclude that analog performance of a downscaled Si-based TFET suffers with gate length down scaling. However, it is worth mentioning that due to absence of CLM, the output resistance and intrinsic gain of Si-based TFET are always higher than corresponding conventional MOS devices, thus indicating its suitability for analog/RF applications.

4 RF PERFORMANCE INVESTIGATION

The variations of RF performance figure of merits are analyzed for different values of channel length. The approximate expression of important RF figure of merits such as, f_T, f_{max} and GBW are given by [17]

$$f_T = \frac{g_m}{2\pi C_{gs}\sqrt{1+2\frac{C_{gd}}{C_{gs}}}} \approx \frac{g_m}{2\pi\left(C_{gd}+C_{gs}\right)} \approx \frac{g_m}{2\pi C_{gg}} \quad (1)$$

$$f_{max} \approx \frac{g_m}{2\pi C_{gs}\sqrt{4\left(R_s+R_i+R_g\right)\left(g_{ds}+g_m\frac{C_{gd}}{C_{gs}}\right)}} \quad (2)$$

$$GBW = \frac{g_m}{20\pi C_{gd}} \quad (3)$$

Where Cgs, Cgd and Cgg denotes gate–to-source, gate-to-drain and total gate capacitance.

From Equations (1) to (3), it is evident that RF Figure-of-Merits (FOMs) depends strongly on parasitic resistances and capacitances. The Miller capacitance ratio denoted by C_{gd}/C_{gs} decreases with gate-length downscaling, thus compensating the higher C_{gd}/C_{gs} obtained from a TFET.

Fig. 8 plots the cut-off frequency f_T as a function V_{GS} for three different channel lengths. It is evident Fig. 10 that gate-length downscaling causes an increase in f_T, due to reduction on parasitic capacitances (C_{gs}+C_{gd}) dominating over the reduction in transconductance g_m.

Fig. 9 shows the variation of maximum frequency of oscillation f_{max} as a function of V_{GS} for three different channel lengths. f_{max} is a transistor extrinsic parameter and depends strongly on parasitic resistances such as R_g, R_i and R_S, where gate resistance R_g equals to 2.6 kΩ for a 20nm thick molybdenum gate material [18]. Moreover, a standard value of Ri equals to 20 nm ohm and RS

equals to 160 ohm is considered in our study as obtained from available literature [19]. Fig. 9 shows that a decrease in channel length causes an increase in f_{max}.

Fig. 10 shows the variation of gain-bandwidth as a function of V_{GS} for two different channel lengths.

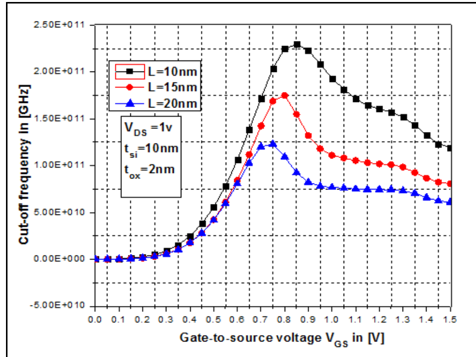

Fig. 8. Variation of Cut-off Frequency (f_T) as a function of Gate-to-source voltage V_{GS} for different Channel Length L = 10 nm, 15 nm, 20 nm with device parameter values V_{DS} = 1 v, t_{Si} = 10 nm and t_{OX} = 3 nm.

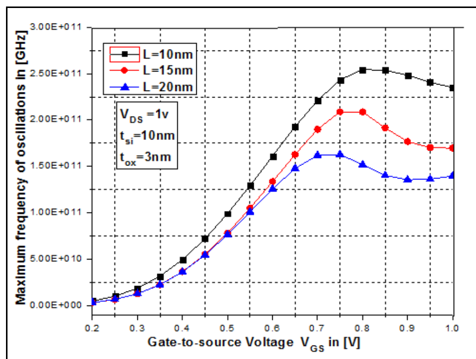

Fig. 9. Variation of maximum frequency of oscillation (f_{max}) as a function of Gate-to-source voltage V_{GS} for different Channel lengths L = 10 nm, 15 nm, 20 nm with device parameter values V_{DS} = 1 v, t_{Si} = 10 nm and t_{OX} = 3 nm.

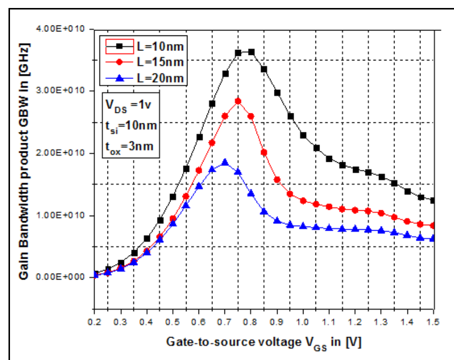

Fig. 10. Variation of Gain Band Width Product (GBW) as a function of Gate-to-source voltage V_{GS} for different channel lengths L = 10 nm, 15 nm, 20 nm with device parameter values V_{DS} = 1 v, t_{Si} = 10 nm and t_{OX} = 3 nm.

GBW strongly depends upon g_m and C_{gd} (gate-to drain capacitance). GBW increases with downscaling. We have obtained a GBW near about 36 GHz and 18 GHz at 10 nm and 20 nm respectively.

5 LINEARITY ANALYSIS

Linearity is one of the important requirements in all RF communication systems. Good linearity gives the minimum contribution of higher order harmonics and inter-modulation terms and results in less distortion at the output RF stage [20].The important device parameters for linearity and analog applications are transconductance and output resistance R_O. The transconductance (g_m) and its derivatives mainly determine the linearity performance of a device [20].

For better linearity performance and suppression of non-linear behavior introduced by g_{m2} and g_{m3}, the optimum bias point is determined by the zero cross over point of g_{m3} (third order derivative of transconductance g_{m1}) where it's value is minimum and there by suppressing the distortion created by g_{m3} . The input power value in dB, at which the gain of the low noise amplifier drops by 1-dB is referred to as 1-dB compression point given by [21-22]

$$1-dB \text{ compression point} = 0.22\sqrt{\frac{g_{m1}}{g_{m3}}} \qquad (4)$$

Where $g_{m1} = \frac{\partial I_{ds}}{\partial V_{gs}}$ and $g_{m3} = \frac{\partial^3 I_{ds}}{\partial V_{gs}^3}$

It is desirable that the Low Noise Amplifier (LNA) should have high –dB compression value for more linearity [20]. High value of 1-dB compression point is necessary for high linearity RF/microwave system to "act linearly".

It is evident from Fig. 11 that channel length reduction results in an increase in the 1-dB compression point owing to the enhanced gate control and hence higher transconductance. Therefore, results reveal that reduction in gate length enhances the device linearity owing to the increasing prominence of velocity saturation resulting in an increasing current driving capability, thereby affecting transconductance and hence, the 1-dB compression point.

Therefore it may be concluded that RF and linearity performance improves with gate-length downscaling in contrast to analog performance which suffers with gate-length downscaling. This clearly indicates trade-off between power efficiency

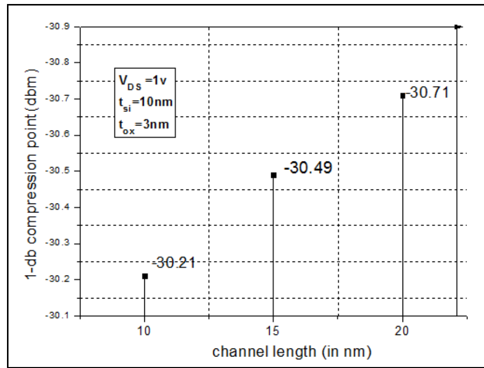

Fig. 11. Variation of 1-dB Compression point (dBm) as a function of V_{GS} for different Channel Length L = 10 nm, 15 nm, 20 nm with device parameter values V_{DS} = 1 v, t_{Si} = 10 nm and t_{OX} = 3 nm.

and bandwidth for possible usage of TFET in low-power analog/RF System-on-chip applications.

6 CONCLUSIONS

This work uncovers the potential benefits of Si-based TFET in the context of RF/analog performance and linearity characteristics. The trends related to their variations as a function of downscaled channel are analyzed. It is observed that maximum TGF of around 70 V^{-1} is found for L = 20 nm. The gain band width (GBW) is near about 36 GHz for L = 10 nm and 18 GHz for L = 20 nm. Thus, in order to use smaller channel lengths for better RF performance and IC scalability, the analog performances suffers. Therefore, it may be concluded that the downscaling of the channel length results in an improvement in RF performance such as f_T and f_{max} and linearity characteristics such as 1-dB compression point. However, the analog performance such as TGF, R_o founds to be degraded with channel-length downscaling.

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